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(71) Applicant *(for all designated States except US)*: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.** [JP/JP]; 1006, OazaKadoma, Kadoma-shi, Osaka 571-8501 (JP).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **DAIGI, Tomoaki** [JP/JP]; 15-7-308, Kakiuchi-cho, Kadoma-shi, Osaka 567-0026 (JP). **KAWAMURA, Hideaki** [JP/JP]; 185-10, Futamachi-cho, Moriyama-shi, Shiga 524-0043 (JP). **KASAHARA, Mitsuhiro** [JP/JP]; 13-17-3, Nagaonishi-machi, Hirakata-shi, Osaka 573-0162 (JP).

(74) Agent: **NAKAJIMA, Shiro**; 6F, Yodogawa 5-Bankan, 2-1, Toyosaki 3-chome, Kita-ku, Osaka-shi, Osaka 531-0072 (JP).

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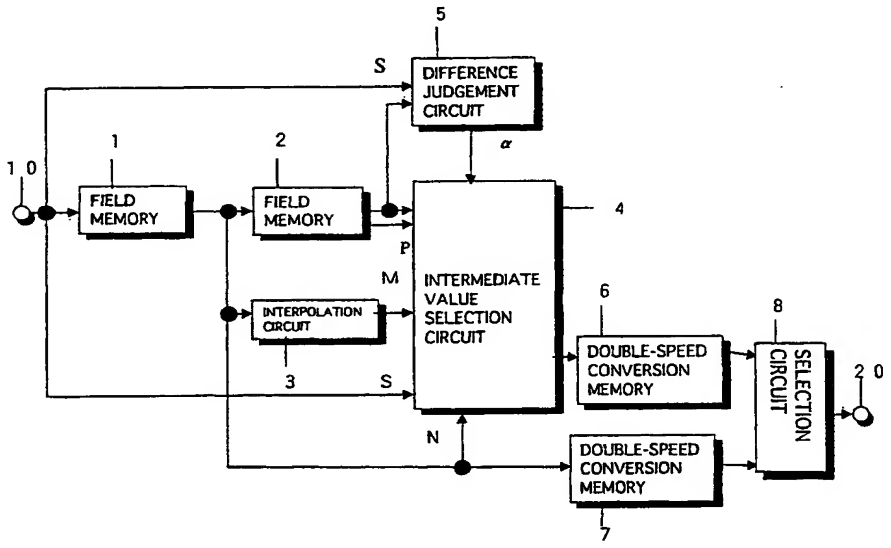

(57) Abstract: An image signal processing apparatus for converting an interlaced image signal to a progressive scanned image signal is provided. Image signals of three fields are acquired for each pixel by delaying each interlaced input image signal using two field memories connected in series. An intermediate signal is selected from the three signals, and intra-field interpolation or inter-field interpolation is performed using one of the signals depending on the selection result. Meanwhile, the difference between the image signals of the preceding and following fields is calculated. If the difference is not smaller than a reference value, the intra-field interpolation is automatically performed without selecting from the two interpolation methods. Such interpolated pixel values and the pixel values of the present field are alternately read at double speed. As a result, the progressive scanned image signal is obtained.

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DESCRIPTION

IMAGE SIGNAL PROCESSING CIRCUIT

TECHNICAL FIELD

The present invention relates to an image signal processing circuit for converting an interlaced image signal to a progressive scanned image signal.

BACKGROUND ART

Motion adaptive scanning line interpolation is known as a scanning line conversion technique for converting an interlaced image signal to a progressive scanned image signal. In motion adaptive scanning line interpolation, motion of an image is detected. When the image is a still image, an interpolated scanning line is generated using an image signal of a field preceding a present field according to inter-field interpolation. When the image is a moving image, an interpolated scanning line is generated using an image signal of the present field according to intra-field interpolation. To perform motion adaptive scanning line interpolation, a large-scale motion detection circuit is necessary.

Japanese Laid-Open Patent Application No. H09-

224223 discloses an image signal processing circuit that can generate favorable images by switching between intra-field interpolation and inter-field interpolation, with no need to employ a motion detection circuit.

FIG. 19 is a block diagram showing an example of such an image signal processing circuit.

The image signal processing circuit shown in the drawing is roughly made up of field memories 21 and 22, an interpolation circuit 23, an intermediate value selection circuit 24, double-speed conversion memories 26 and 27, and a selection circuit 28.

An interlaced image signal is input in an input terminal 10. The input image signal is then output to the field memory 21 and the intermediate value selection circuit 24. The field memory 21 outputs the image signal after a delay of one field. The image signal output from the field memory 21 is passed to the field memory 22, the interpolation circuit 23, and the double-speed conversion memory 27. The field memory 22 outputs the image signal passed from the field memory 21, after a delay of one field.

Suppose an image signal output from the field memory 21 is an image signal of the *n*th field. Then an image signal input in the input terminal 10 is an image signal of the *(n+1)*th field, and an image signal output from the field memory 22 is an image signal of the *(n-1)*th field.

Here, *n* is a positive integer.

The interpolation circuit 23 generates an interpolation signal from pixels in the *n*th field, using the image signal of the *n*th field passed from the field memory 21.

The intermediate value selection circuit 24 receives the image signal output from the field memory 22, the interpolation signal generated by the interpolation circuit 23, and the image signal input in the input terminal 10. Here, let *A* be a pixel value of the image signal output from the field memory 22, *B* be a pixel value of the interpolation signal output from the interpolation circuit 23, and *C* be a pixel value of the image signal input in the input terminal 10.

The intermediate value selection circuit 24 compares pixel values *A*, *B*, and *C* for each pixel period. The intermediate value selection circuit 24 selects an intermediate value from pixel values *A*, *B*, and *C*, and outputs the selected pixel value to the double-speed conversion memory 26. Thus, pixel values output from the intermediate value selection circuit 24 are sequentially stored in the double-speed conversion memory 26. Meanwhile, pixel values of image signals input in the input terminal 10 are sequentially stored in the double-speed conversion memory 27.

FIG. 20 shows conditions used by the intermediate value selection circuit 24 to determine an intermediate value. As shown in the drawing, pixel value *A* is selected when $C \geq A > B$ or $B \geq A > C$. Pixel value *B* is selected when $A > B > C$ or $C \geq B \geq A$. Pixel value *C* is selected when $A > C \geq B$ or $B > C \geq A$.

The selection circuit 28 alternately reads the pixel values from the double-speed conversion memory 26 and the pixel values from the double-speed conversion memory 27 and outputs them to an output terminal 20, in a period which is half the pixel period of the image signal input in the input terminal 10. As a result, a progressive scanned image signal is obtained in the output terminal 20.

Thus, when pixel value *A* of the *(n-1)*th field is judged as being an intermediate value, an interpolated scanning line is generated by inter-field interpolation using the image signal of the *(n-1)*th field. When pixel value *B* is judged as being an intermediate value, an interpolated scanning line is generated by intra-field interpolation using the image signal of the *n*th field. When pixel value *C* of the *(n+1)*th field is judged as being an intermediate value, an interpolated scanning line is generated by inter-field interpolation using the image signal of the *(n+1)*th field.

The aforementioned patent application also

discloses a method of inter-field interpolation that uses vertical components of high frequencies in the image signal of the preceding or following field. In this specification, the term "vertical high-frequency components" means that values of pixels which are adjacent in the vertical direction vary greatly, i.e. that the spatial frequency is high.

A specific example of this inter-field interpolation method that uses vertical high-frequency components is explained below, with reference to FIGS. 21 and 22.

FIG. 21 shows pixels of the *(m-1)*th line, *m*th line, and *(m+1)*th line in each of the *(n-1)*th, *n*th, and *(n+1)*th fields across a time axis (a horizontal axis). Circles in solid line represent pixels which exist in interlaced images, whereas circles in broken line represent pixels which do not exist in the interlaced images. The pixels of the *n*th field are shifted from the pixels of the *(n-1)*th field and the pixels of the *(n+1)*th field by half the line width, which is the property of interlacing.

In the drawing, *PC*, *PB*, and *PA* denote the values of the pixels of the *(m-1)*th, *m*th, and *(m+1)*th lines in the *(n-1)*th field, respectively. *MD*, *MC*, *MB*, and *MA* denote the values of the pixels of the *(m-1)*th, *m*th, *(m+1)*th, and *(m+2)*th lines in the *n*th field, respectively. *SC*, *SB*, and *SA* denote the values of the pixels of the *(m-1)*th,

*m*th, and *(m+1)*th lines in the *(n+1)*th field, respectively. Note that *m* is a positive integer.

The following explanation deals with the case where a pixel shown by a diagonally shaded circle in the *n*th field is interpolated. In the drawing, *IN* denotes the value of the pixel to be interpolated (hereafter referred to as an "interpolation pixel value").

First, pixel value *PB* of the *(n-1)*th field, interpolation value *M* of the *n*th field, and pixel value *SB* of the *(n+1)*th field are compared to select an intermediate value. Based on this selection, one of the following interpolation values *a*, *b*, and *c* is selected as interpolation pixel value *IN*. Note here that *M=(MB+MC)/2*.

Interpolation values *a*, *b*, and *c* are calculated from the following equations.

$$a=\{2\times PB-(PA+PC)\}/4+\{1\times(MA+MD)+5\times(MB+MC)\}/12 \quad \cdots\cdots \text{(Equation 1)}$$

$$b=(MB+MC)/2 \quad \cdots\cdots \text{(Equation 2)}$$

$$c=\{2\times SB-(SA+SC)\}/4+\{1\times(MA+MD)+5\times(MB+MC)\}/12 \quad \cdots\cdots \text{(Equation 3)}$$

FIG. 22 shows conditions for determining an intermediate value in the scanning line interpolation shown in FIG. 21. As illustrated, interpolation value *a* is selected as interpolation pixel value *IN* when $SB \geq PB > M$ or $M \geq PB > SB$. Interpolation value *b* is selected as interpolation pixel value *IN* when $PB > M > SB$ or $SB \geq M \geq PB$. Interpolation value *c* is selected as interpolation pixel value *IN* when $PB > SB \geq M$ or $M > SB \geq PB$.

Which is to say, when pixel value *PB* of the *(n-1)*th field is judged as being an intermediate value, interpolation value *a* is selected as interpolation pixel value *IN*. When interpolation value *M* of the *n*th field is judged as being an intermediate value, interpolation value *b* is selected as interpolation pixel value *IN*. When pixel value *SB* of the *(n+1)*th field is judged as being an intermediate value, interpolation value *c* is selected as interpolation pixel value *IN*. Here, the first term of the right side of the Equation 1 is $\{2 \times PB - (PA+PC)\}$. This being so, if $PA=PB=PC$, the calculation outcome is *0*. In other words, the first term of Equation 1 has the following property. If values of pixels adjacent in the vertical direction do not vary greatly, the calculation outcome is small. If, on the other hand, the values of the adjacent pixels vary greatly, the calculation outcome is large. That is to say, high-frequency components result in a

larger calculation outcome than low-frequency components. The same applies to the first term of Equation 3, where high-frequency components result in a larger calculation outcome.

The reason for employing such an inter-field interpolation method whereby interpolation pixel value *IN* is affected to a greater extent when the absolute values of vertical high-frequency components are larger in the preceding or following field is given below. A moving image has high-frequency components. Accordingly, if the spatial frequency of an image which contains the pixel selected as the intermediate value is high, reflecting such a spatial frequency upon the interpolation pixel value makes the resulting image appear to change naturally with time. When interpolating horizontal scanning lines as in the case of interpolation from interlacing to progressive scanning, movement in the horizontal direction is not a concern, so long as movement in the vertical direction is taken into account. Hence it is rational to perform interpolation using vertical high-frequency components.

However, the inventors of the present application found that this interpolation method can cause the occurrence of noise in some particular cases. A specific example of this is given below.

Suppose pixel values *PA*, *MA*, *MB*, *MC*, *MD*, *SA*, and *SC* are *100*, pixel value *SB* is *50*, pixel value *PB* is *10*, and pixel value *PC* is *0*. The *n*th field is an image in which each pixel has the same pixel value. In this case, interpolation value *M* is *100*. Since *PB*<*M*, *PB*<*SB*, and *M*>*SB*, interpolation value *c* is selected as interpolation pixel value *IN*, which is expressed as follows:

$$IN=c=\{2\times50-(100+100)\}/4$$
$$+\{1\times(100+100)+5\times(100+100)\}/12=75$$

This value greatly differs with the desired output value *100*. As a result, noise appears in the resulting progressive scanned image. This is caused by the following reason. Since the above image signal processing circuit does not use a motion detection circuit, inter-field interpolation is performed even when the movement of the input image signal is large.

DISCLOSURE OF INVENTION

The present invention was conceived in view of the problem described above, and has a primary object of providing an image signal processing circuit that can perform inter-field interpolation while minimizing the occurrence of noise.

The stated object can be achieved by an image signal processing apparatus for converting an image signal of a first scanning format to an image signal of a second scanning format, including: a main interpolating unit for interpolating a scanning line between any two adjacent scanning lines in a present field that corresponds to the image signal of the first scanning format, by selectively executing two interpolation methods for each target pixel which constitutes the scanning line to be interpolated, the two interpolation methods being inter-field interpolation that uses pixels of a field preceding the present field and a field following the present field, and intra-field interpolation that uses pixels in the present field which are in a neighborhood of the target pixel; a change detecting unit for detecting a change of an image, by referring to an image signal of the preceding field and an image signal of the following field; an automatic interpolating unit for prohibiting, depending on a detection result obtained by the change detecting unit, the main interpolating unit to select and execute one of the two interpolation methods, and instead automatically executing a specific interpolation method; and an image signal outputting unit for alternately outputting scanning lines of the image signal of the present field and interpolated scanning lines obtained

by the combination of the main interpolating unit, the change detecting unit, and the automatic interpolating unit.

Here, the change detecting unit may detect an extent to which the image changes with time, wherein the automatic interpolating unit automatically executes the intra-field interpolation, when the detected extent is greater than a reference value.

Here, the first scanning format may be interlace scanning, and the second scanning format progressive scanning, wherein the image signal outputting unit outputs a progressive scanned image signal of one frame, responsive to an interlaced image signal of one field.

Here, the change detecting unit may calculate a difference between a value of a pixel in the preceding field that positionally corresponds to the target pixel and a value of a pixel in the following field that positionally corresponds to the target pixel, and judge whether the difference is greater than the reference value.

Here, when the present field is an *n*th field, the preceding field may be an *(n-1)*th field and the following field an *(n+1)*th field, wherein the main interpolating unit is equipped with a series circuit of at least two field memories, and when the image signal of the *(n+1)*th

field is being input in a field memory of a first stage in the series circuit, the image signal of the *n*th field is being output from the field memory of the first stage and the image signal of the *(n-1)*th field is being output from a field memory of a second stage in the series circuit.

Here, the main interpolating unit may include: an intermediate value selecting unit for selecting an intermediate value from (a) the value of the pixel in the *(n-1)*th field that positionally corresponds to the target pixel, (b) the value of the pixel in the *(n+1)*th field that positionally corresponds to the target pixel, and (c) an average value of pixels in the *n*th field that are adjacent to the target pixel, the intermediate value being smaller than one of remaining two values but greater than a different one of the remaining two values; a first inter-field interpolating unit for obtaining high-frequency components from values of pixels in the *(n-1)*th field that are made up of the pixel positionally corresponding to the target pixel and neighboring pixels thereof, and calculating a first interpolation value for the target pixel using the high-frequency components; a second inter-field interpolating unit for obtaining high-frequency components from values of pixels in the *(n+1)*th field that are made up of the pixel positionally corresponding to the target pixel and neighboring pixels

thereof, and calculating a second interpolation value for the target pixel using the high-frequency components; an intra-field interpolating unit for calculating a third interpolation value for the target pixel, using an average value of the pixels in the *n*th field that are in the neighborhood of the target pixel; and a selecting unit for selecting one of the first inter-field interpolating unit, the second inter-field interpolating unit, and the intra-field interpolating unit based on the intermediate value selected by the intermediate value selecting unit, and outputting an interpolation value calculated by the selected interpolating unit to the image signal outputting unit as a pixel value of the target pixel.

Here, the reference value may be set at a value in a range of *7* to *16*, when the image is expressed in *256* levels of gray.

Here, the change detecting unit may calculate a difference between an average value of a pixel group in the preceding field and an average value of a pixel group in the following field, and judge whether the difference is greater than the reference value, each pixel group being made up of a pixel that positionally corresponds to the target pixel and neighboring pixels thereof.

Here, the image signal processing apparatus may further include: an edge detecting unit for detecting an

edge in the preceding field or the following field, the edge being parallel to a scanning line that includes a pixel positionally corresponding to the target pixel; and a stopping unit for temporarily stopping the automatic interpolating unit from prohibiting the main interpolating unit, when the edge detecting unit detects the edge.

The stated object can also be achieved by an image signal processing apparatus for converting an image signal of a first scanning format to an image signal of a second scanning format, including: a main interpolating unit for interpolating a scanning line between any two adjacent scanning lines in a present field that corresponds to the image signal of the first scanning format, by selectively executing inter-field interpolation and intra-field interpolation to calculate a first interpolation value for each target pixel which constitutes the scanning line to be interpolated, the inter-field interpolation using pixels of a field preceding the present field and a field following the present field, and the intra-field interpolation using pixels in the present field that are in a neighborhood of the target pixel; a sub-interpolating unit for executing the intra-field interpolation to calculate a second interpolation value for the target pixel, using

the pixels in the present field that are in the neighborhood of the target pixel; a change detecting unit for detecting a change of an image, by referring to an image signal of the preceding field and an image signal of the following field; a weight setting unit for setting a first weight by which the first interpolation value should be multiplied, and a second weight by which the second interpolation value should be multiplied; a weighting/adding unit for multiplying, depending on a detection result obtained by the change detecting unit, the first interpolation value by the first weight and the second interpolation value by the second weight, and calculating a sum of the weighted first interpolation value and the weighted second interpolation value, the sum being set as a value of the target pixel; and an image signal outputting unit for alternately outputting scanning lines of the image signal of the present field and interpolated scanning lines obtained by the combination of the main interpolating unit, the sub-interpolating unit, the change detecting unit, the weight setting unit, and the weighting/adding unit.

Here, the weight setting unit may set the first weight and the second weight, in accordance with the difference obtained for the target pixel and differences obtained for pixels in the present field that are subjected

to interpolation and are in a neighborhood of the target pixel.

Here, the weight setting unit may set the first weight and the second weight, in accordance with the difference calculated by the change detecting unit.

The stated object can also be achieved by an image signal processing apparatus for interpolating necessary scanning lines, when converting an interlaced image signal to a progressive scanned image signal, including: a first interpolating circuit for generating an interpolation value *M* for each target pixel which constitutes a scanning line to be interpolated in an *n*th field that corresponds to the interlaced image signal, by performing interpolation within the *n*th field; an intermediate value selecting circuit for selecting an intermediate value from (a) a value *P* of a pixel in an *(n-1)*th field that positionally corresponds to the target pixel, (b) a value *S* of a pixel in an *(n+1)*th field that positionally corresponds to the target pixel, and (c) the interpolation value *M*, the intermediate value being smaller than one of remaining two values but greater than a different one of the remaining two values; a difference judging circuit for calculating a difference ΔL using an image signal of the *(n-1)*th field and an image signal of the *(n+1)*th field, and outputting a judgement result based

on a comparison between the difference ΔL and a reference value R; and a target pixel generating circuit for outputting, as a value of the target pixel, (a) the interpolation value M, when the difference judging circuit judges $\Delta L \geq R$ or the intermediate value selecting circuit selects the interpolation value M, (b) a first interpolation value for the target pixel which is generated by performing first inter-field interpolation that uses at least the image signal of the $(n-1)$th field, when the difference judging circuit judges $\Delta L < R$ and the intermediate value selecting circuit selects the value P, and (c) a second interpolation value for the target pixel which is generated by performing second inter-field interpolation that uses at least the image signal of the $(n+1)$th field, when the difference judging circuit judges $\Delta L < R$ and the intermediate value selecting circuit selects the value S.

Here, the target pixel generating circuit may include: a first high-frequency component extracting circuit for extracting high-frequency components from pixels in the $(n-1)$th field which are consecutive in a vertical direction; a second high-frequency component extracting circuit for extracting high-frequency components from pixels in the $(n+1)$th field which are consecutive in the vertical direction; a second

interpolating circuit for generating a third interpolation value for the target pixel, by performing interpolation within the *n*th field; a first calculating circuit for performing a calculation, using the high-frequency components extracted by the first high-frequency component extracting circuit and the third interpolation value; and a second calculating circuit for performing a calculation, using the high-frequency components extracted by the second high-frequency component extracting circuit and the third interpolation value, wherein a result of the calculation by the first calculating circuit is the first interpolation value, whereas a result of the calculation by the second calculating circuit is the second interpolation value.

The stated object can also be achieved by an image signal processing apparatus for interpolating necessary scanning lines, when converting an interlaced image signal to a progressive scanned image signal, including: a first interpolating circuit for generating an interpolation value *M* for each target pixel which constitutes a scanning line to be interpolated in an *n*th field that corresponds to the interlaced image signal, by performing interpolation within the *n*th field; an intermediate value selecting circuit for selecting an intermediate value from (a) a value *P* of a pixel in an

*(n-1)*th field that positionally corresponds to the target pixel, (b) a value *S* of a pixel in an *(n+1)*th field that positionally corresponds to the target pixel, and (c) the interpolation value *M*, the intermediate value being smaller than one of remaining two values but greater than a different one of the remaining two values; a difference judging circuit for calculating a difference ΔL using an image signal of the *(n-1)*th field and an image signal of the *(n+1)*th field, and outputting a judgement result based on a comparison between the difference ΔL and a reference value *R*; a first high-frequency component extracting circuit for extracting high-frequency components from pixels in the *(n-1)*th field which are consecutive in a vertical direction; a second high-frequency component extracting unit for extracting high-frequency components from pixels in the *(n+1)*th field which are consecutive in the vertical direction; a second interpolating circuit for generating a first interpolation value for the target pixel, by performing interpolation within the *n*th field; a first calculating circuit for performing a calculation, using the high-frequency components extracted by the first high-frequency component extracting circuit and the first interpolation value; a second calculating circuit for performing a calculation, using the high-frequency components extracted by the second high-frequency

component extracting circuit and the first interpolation value; a selecting circuit for selecting and outputting (a) the interpolation value *M*, when the intermediate value selecting circuit selects the interpolation value *M*, (b) a result of the calculation by the first calculating circuit, when the intermediate value selecting circuit selects the value *P*, and (c) a result of the calculation by the second calculating circuit, when the intermediate value selecting circuit selects the value *S*; a third interpolating circuit for generating a second interpolation value for the target pixel, by performing interpolation within the *n*th field; a weight setting circuit for setting a first weight by which an output value of the selecting circuit should be multiplied and a second weight by which the second interpolation value should be multiplied, according to the judgement result by the difference judging circuit; and a weighting/adding circuit for multiplying the output value of the selecting circuit by the first weight and the second interpolation value by the second weight, and outputting a sum of the weighted values as a value of the target pixel.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 shows an image signal processing circuit to which the first embodiment of the present invention

relates.

FIG. 2 shows a construction of a difference judgement circuit shown in FIG. 1.

FIG. 3 shows a detailed construction of an intermediate value selection circuit shown in FIG. 1.

FIG. 4 shows a specific example of an intermediate value judgement circuit shown in FIG. 3.

FIG. 5 is a truth table used for a selection operation by a selection circuit shown in FIG. 3.

FIG. 6 shows an example image subjected to an interpolation operation.

FIG. 7 shows a pixel pattern of each field of the image shown in FIG. 6.

FIG. 8 shows another example image subjected to an interpolation operation.

FIG. 9 shows a pixel pattern of each field of the image shown in FIG. 8.

FIG. 10 shows another example image subjected to an interpolation operation.

FIG. 11 shows a pixel pattern of each field of the image shown in FIG. 10.

FIG. 12 shows an image signal processing circuit to which the second embodiment of the invention relates.

FIG. 13 shows a specific construction of an intermediate value selection circuit shown in FIG. 12.

FIG. 14 shows an example of weighting by a weighting factor setting circuit shown in FIG. 12.

FIG. 15 shows an image signal processing circuit to which the third embodiment of the invention relates.

FIG. 16 illustrates the principle of edge detection.

FIG. 17 shows an image for which interpolation of the third embodiment is effective.

FIG. 18 shows an interpolation operation performed on the image shown in FIG. 17.

FIG. 19 shows a conventional image signal processing circuit.

FIG. 20 is a table showing the conditions of judging an intermediate value by an intermediate value selection circuit shown in FIG. 19.

FIG. 21 shows pixels of three fields which are subjected to an interpolation operation of the image signal processing circuit shown in FIG. 19.

FIG. 22 shows the conditions of judging an intermediate value in the interpolation shown in FIG. 21.

BEST MODE FOR CARRYING OUT THE INVENTION

(First Embodiment)

FIG. 1 shows a construction of an image signal processing circuit which is the first embodiment of the present invention. This image signal processing circuit

is roughly made up of field memories 1 and 2, an interpolation circuit 3, an intermediate value selection circuit 4, a difference judgement circuit 5, double-speed conversion memories 6 and 7, and a selection circuit 8.

An interlaced image signal is input in an input terminal 10. The input image signal is passed to the field memory 1, the intermediate value selection circuit 4, and the difference judgement circuit 5.

The field memories 1 and 2 and the interpolation circuit 3 are the same as those explained in the background art, though they are briefly explained once again.

The field memory 1 outputs the image signal after a delay of one field. The output image signal is synchronous with the input image signal, with the corresponding pixels being output one at a time. The image signal output from the field memory 1 is supplied to the field memory 2, the interpolation circuit 3, the intermediate value selection circuit 4, and the double-speed conversion memory 7 pixel by pixel in the output order. The field memory 2 has the same construction as the field memory 1, and outputs the input image signal after a delay of one field. Suppose an image signal output from the field memory 1 is an image signal of the *n*th field. Then an image signal input in the input terminal 10 is an image signal of the *(n+1)*th field, and

an image signal output from the field memory 2 is an image signal of the *(n-1)*th field. Here, *n* is a positive integer.

The interpolation circuit 3 generates an interpolation signal from pixels of the *n*th field, using the image signal of the *n*th field given from the field memory 1. The intermediate value selection circuit 4 is given the image signal output from the field memory 2, the interpolation signal generated by the interpolation circuit 3, and the image signal input in the input terminal 10. The pixels which are simultaneously input in the intermediate value selection circuit 4 are pixels of the different fields which are located at the same pixel position on a screen.

Let *P* be a pixel value of the image signal output from the field memory 2, *M* be a pixel value of the interpolation signal (such a pixel value is hereafter referred to as an "interpolation value") output from the interpolation circuit 3, *S* be a pixel value of the image signal input in the input terminal 10, and *N* be a pixel value of the image signal output from the field memory 1.

The difference judgement circuit 5 receives image signal *S* of the *(n+1)*th field from the input terminal 10, and image signal *P* of the *(n-1)*th field from the field

memory 2. The difference judgement circuit 5 calculates the difference between the values of the corresponding pixels in both fields, and compares the difference with a reference value stored therein. The difference judgement circuit 5 then outputs comparison result α. When the difference is equal to or greater than the reference value, $\alpha=1$. When the difference is smaller than the reference value, $\alpha=0$. The difference judgement circuit 5 can be made up of a subtractor and a comparator, as shown in FIG. 2. The subtractor calculates absolute value ($|S-P|$) of the difference between the corresponding pixel values of image signal S of the $(n+1)$th field and image signal P of the $(n-1)$th field. The comparator compares the absolute value output from the subtractor, with reference value R given to a comparison terminal. The comparator then outputs comparison result α. As reference value R, an adequate value is selected from 7 to 16 for instance. It should be noted that this value is limited to the case where an image is expressed in 256 ($=2^8$) levels of gray. Therefore, a different reference value should be used if the total number of gray levels is different. A method of setting the reference value is explained in more detail later.

The intermediate value selection circuit 4 performs two types of operations, depending on the value of

comparison result α. If $\alpha=0$, the intermediate value selection circuit 4 compares pixel value P, interpolation value M, and pixel value S for each pixel period, and judges which of P, M, and S is an intermediate value. The intermediate value selection circuit 4 selects inter-field interpolation or intra-field interpolation based on the judgement result, and outputs interpolation pixel value IN. If $\alpha=1$, on the other hand, the intermediate value selection circuit 4 automatically performs intra-field interpolation, without comparing the pixel values. The result of this interpolation is output as interpolation pixel value IN. A construction of this intermediate value selection circuit 4 is shown in FIG. 3, which is explained in greater detail later.

The double-speed conversion memory 6 sequentially stores interpolation pixel values IN output from the intermediate value selection circuit 4. Meanwhile, the double-speed conversion memory 7 sequentially stores pixel values N of image signals output from the field memory 1. The double-speed conversion memories 6 and 7 each have at least two line memories. In each of the double-speed conversion memories 6 and 7, an operation in which a pixel value (or an interpolation pixel value) is written in one line memory while a pixel value (or an interpolation pixel value) written in the other line

memory is read can be performed alternately on the line memories.

The selection circuit 8 alternately reads interpolation pixel values *IN* of one readable line from the double-speed conversion memory 6, and pixel values *N* of one readable line from the double-speed conversion memory 7. The speed of reading one pixel is half the pixel period of the image signal input in the input terminal 10. As a result, a progressive scanned image signal is obtained in an output terminal 20. The selection circuit 8 can be realized by a multiplexer (not shown in the drawing).

FIG. 3 is a block diagram showing a construction of the intermediate value selection circuit 4 in the image signal processing circuit of FIG. 1. As shown in the drawing, the intermediate value selection circuit 4 includes an intermediate value judgement circuit 30, vertical high-pass filters 31 and 32, adders 33 and 34, an interpolation circuit 35, and a selection circuit 36.

The intermediate value judgement circuit 30 receives pixel value *P* of the image signal of the *(n-1)*th field output from the field memory 2 shown in FIG. 1, interpolation value *M* of the interpolation signal output from the interpolation circuit 3, and pixel value *S* of the image signal of the *(n+1)*th field input in the input

terminal 10.

The intermediate value judgement circuit 30 compares pixel value *P* of the image signal of the *(n-1)*th field, intra-field interpolation value *M* of the *n*th field, and pixel value *S* of the image signal of the *(n+1)*th field, to judge which of *P*, *M*, and *S* is an intermediate value. The intermediate value judgement circuit 30 outputs the judgement result to the selection circuit 36. A specific example of the intermediate value judgement circuit 30 is shown in FIG. 4. In the drawing, judgement circuits 211a-211c judge the inequality of any two values out of three image signals *P*, *M*, and *S*. AND circuits 212a-212f determine the inequality of three image signals *P*, *M*, and *S* based on the judgement result of each judgement circuit. OR circuits 213a-213c output an intermediate value selected from image signals *P*, *M*, and *S*.

The vertical high-pass filter 31 shown in FIG. 3 is given pixel value *S* of the image signal of the *(n+1)*th field from the input terminal 10, whereas the vertical high-pass filter 32 is given pixel value *P* of the image signal of the *(n-1)*th field from the field memory 2.

The vertical high-pass filter 31 extracts vertical high-frequency components of the image signal of the *(n+1)*th field. The vertical high-pass filter 32 extracts vertical high-frequency components of the image signal

of the *(n-1)*th field. The vertical high-pass filters 31 and 32 are realized by circuits that compute the first terms of the right sides of Equations 3 and 1 shown in the background art, using, for instance, values of three vertically-adjacent pixels in the image signals of the *(n+1)*th and *(n-1)*th fields.

The interpolation circuit 35 generates an interpolation value, by performing interpolation using vertically-adjacent pixels in the image signal of the *n*th field output from the field memory 1. The interpolation circuit 35 can be realized by a circuit that computes the second terms of the right sides of Equations 1 and 3. The term "vertical high-frequency component" has been defined in the description of the background art.

The adder 33 weights the output value of the vertical high-pass filter 32 and the interpolation value output from the interpolation circuit 35. The adder 33 then adds the weighted output value and interpolation value, and outputs the sum to the selection circuit 36 as interpolation value *a*. The adder 34 weights the output value of the vertical high-pass filter 31 and the interpolation value output from the interpolation circuit 35. The adder 34 then adds the weighted output value and interpolation value, and outputs the sum to the selection circuit 36 as interpolation value *c*. Also, interpolation

value *M* output from the interpolation circuit 3 shown in FIG. 1 is input to the selection circuit 36 as interpolation value *b*. As can be understood from FIG. 3, interpolation values *a*, *b*, and *c* are given by Equations 1, 2, and 3 shown in the background art.

The selection circuit 36 selects one of interpolation value *a* output from the adder 33, interpolation value *b* output from the interpolation circuit 3, and interpolation value *c* output from the adder 34, based on the judgement result of the intermediate value judgement circuit 30 and judgement result α of the difference judgement circuit 5. The selection circuit 36 outputs the selected interpolation value as interpolation pixel value *IN*.

As shown in a truth table of FIG. 5, if the intermediate value judgement circuit 30 judges pixel value *P* as being an intermediate value and if $\alpha=0$, the selection circuit 36 outputs interpolation value *a* as interpolation pixel value *IN*. If the intermediate value judgement circuit 30 judges interpolation value *M* as being an intermediate value or if $\alpha=1$, the selection circuit 36 outputs interpolation value *b* as interpolation pixel value *IN*. If the intermediate value judgement circuit 30 judges pixel value *S* as being an intermediate value and if $\alpha=0$, the selection circuit 36 outputs interpolation

value *c* as interpolation pixel value *IN*.

Thus, when pixel value *P* of the image signal of the *(n-1)*th field is judged as being an intermediate value and the difference between the image signals of the *(n-1)*th and *(n+1)*th fields is below the reference value, interpolation pixel value *IN* is generated by inter-field interpolation that uses the vertical high-frequency components of the image signal of the *(n-1)*th field. When interpolation value *M* is judged as being an intermediate value or the difference between the image signals of the *(n-1)*th and *(n+1)*th fields is equal to or greater than the reference value, interpolation pixel value *IN* is generated by intra-field interpolation that uses the image signal of the *n*th field. When pixel value *S* of the image signal of the *(n+1)*th field is judged as being an intermediate value and the difference between the image signals of the *(n-1)*th and *(n+1)*th fields is below the predetermined value, interpolation pixel value *IN* is generated by inter-field interpolation that uses the vertical high-frequency components of the image signal of the *(n+1)*th field.

An interpolation operation performed by the image signal processing circuit with the above construction is explained using specific examples below. FIG. 6 shows an image in which a black-colored strip area runs between

a gray-colored area and a white-colored area in a slanting direction. It is assumed that the gray level of the gray-colored area is *128*, the gray level of the white-colored area is *255*, and the gray level of the black-colored area is *0*. The image is moving to the right by two pixels per field.

This image is interpolated in the following manner. The reference value used in the difference judgement circuit 5 is set at 7 for the sake of convenience.

In FIG. 6, an area enclosed with a broken-line box is a vertical line of interest in the *n*th field. Since the image is moving to the right by one pixel per field, a vertical line of interest which is located at the same position in the preceding field is a set of pixels enclosed by a solid-line box in FIG. 7(a). Note that pixels shown by broken-line circles do not actually exist in these fields, since the image is an interlaced image.

Likewise, a vertical line of interest that is located at the same position in the following field is a set of pixels enclosed by a solid-line box in FIG. 7(c). FIG. 7(b) shows the vertical line of interest in the *n*th field, where *IN* denotes a pixel to be interpolated. Here, difference *(|SB-PB|)* of the values of the pixels in the *(n+1)*th and *(n-1)*th fields which are located at the same position as the pixel to be interpolated is *|128-255|=127*.

Since $127>7$ (7 being reference value R), $\alpha=1$. In this case, interpolation pixel value IN is determined using pixel values of the vertical line of interest in the nth field according to Equation 2, so that $IN=0$.

This interpolation result correlates well with the original image of FIG. 6, indicating that appropriate interpolation was carried out. If the conventional interpolation technique is used, on the other hand, the intermediate value is 128 and interpolation pixel value IN is determined using Equation 3, so that $IN=63$. This causes the occurrence of noise, indicating that the interpolation was not successful.

The above example deals with the case where the image that slants from the top right to the bottom left is moving to the right. However, favorable interpolation can also be performed in the case where the same image is moving to the left. Likewise, favorable interpolation can be performed in the case where an image that slants from the top left to the bottom right is moving to the right or to the left. These effects can be obtained because whenever the difference between pixel value PB of the $(n-1)$th field and pixel value SB of the $(n+1)$th field is equal to or greater than the reference value, $\alpha=1$ is set and intra-field interpolation is automatically performed regardless of which field the intermediate value belongs

to. In other words, when the temporal change of the value of the pixel at the same position is large, intra-field interpolation is executed so as to produce a natural-looking image that changes smoothly.

The following explains interpolation performed on other two types of images, to further examine the effects of this embodiment.

FIG. 8 shows an image that sharply slants from the top right to the bottom left. This image is moving to the left by one pixel per field. This being so, vertical lines of interest in the $(n-1)$th, nth, and $(n+1)$th fields are shown by solid-line boxes in FIGS. 9(a) to 9(c). From this drawing, $|PB-SB|=127>7$ (7 being reference value R), so that $\alpha=1$. Hence intra-field interpolation is performed in this case too, which produces a favorable interpolated image.

FIG. 10 shows an image that slants from the top left to the bottom right with a relatively gentle slope (by one pixel in the vertical direction against three pixels in the horizontal direction). This image is moving to the left by six pixels per field. This being so, vertical lines of interest in the $(n-1)$th, nth, and $(n+1)$th fields are shown by solid-line boxes in FIGS. 11(a) to 11(c). In this case too, $\alpha=1$, so that intra-field interpolation is performed which produces a favorable interpolated

image.

On the other hand, if the conventional technique is used to interpolate the image of FIG. 8 or 10, the pixel of the *(n-1)*th or *(n+1)*th field is set as an intermediate value, so that inter-field interpolation that uses the high-frequency components of the image signal of the *(n-1)*th or *(n+1)*th field is performed. The result of such interpolation is obviously not *0*. This causes the occurrence of noise, unlike the present embodiment.

As can be seen from the examples shown in FIGS. 8 and 10, when a slope of an image is gentler, by increasing the moving speed of the image in the horizontal direction the pixel patterns of the vertical lines of interest in the *(n-1)*th, *n*th, and *(n+1)*th fields become identical, as a result of which the interpolation conditions become the same. In such a case, if the slope is equal to or greater than one pixel in the vertical direction against *k* pixels in the horizontal direction, noise occurs when the conventional interpolation technique is used.

A method of setting the reference value in the difference judgement circuit 5 is explained below. Reference value *R* in the difference judgement circuit 5 is used to judge whether the input image signal is a still image or a moving image. Therefore, if there is even a slight inter-frame difference, it is fundamentally

desirable to treat the image signal as a moving image. However, when the image is expressed in 256 levels of gray, the image can be judged as being a still image if the difference is 3 to 4 which is a little higher than 1% of the total gray scale. In reality, however, noise is usually present in the image signal, so that the difference tends to be still larger even when the image is a complete still image. Consider noise in accordance with a normal distribution with mean value of 0 and standard deviation of σ. When the image signal is expressed in 256 levels of gray as in this embodiment, σ is typically about 2 to 4. In accordance with the normal distribution, the probability of the noise being $-\sigma$ to $+\sigma$ is 68.27%, the probability of the noise being $-2\times\sigma$ to $2\times\sigma$ is 95.45%, and the probability of the noise being $-3\times\sigma$ to $3\times\sigma$ is 99.73%. This being the case, if the difference is larger than 2 σ or 3 σ by a little more than 1% of the total gray scale, it is preferable to judge the image as being a moving image, rather than judging that the image contains noise. Therefore, if σ is 2 to 4, $2\times\sigma$ is 4 to 8 and $3\times\sigma$ is 6 to 12. Hence reference value R is preferably 7 to 16, which can be obtained by adding 3 to 4 that are a little higher than 1% of the total gray scale to the values of 2 σ to 3 σ, i.e. 4 to 12.

Note that if the S/N ratio (the value of σ) of each

input image signal is known, reference value *R* can be optimally set for each individual signal according to the above calculations. Here, a small value is set when the *S/N* ratio is high, whereas a large value is set when the *S/N* ratio is low.

Also, while in this embodiment the inter-frame difference is calculated as the difference between one pixel of the *(n-1)*th field and one pixel of the *(n+1)*th field, instead the difference calculated using the average value of the pixel and its neighboring pixels of each of the two fields may be compared with reference value *R*. In such a case, when *j* denotes the number of pixels used to calculate the average, the mean value of noise in the average is unchanged at *0*. When the above σ is used, the standard deviation is $\sigma/sqrt(j)$ (*sqrt(j)* is the square root of *j*). if *j=9*, the standard deviation is σ /3. Accordingly, when σ is *2* to *4*, $2\times\sigma$ is *1* to *2* and $3\times\sigma$ is *2* to *4*. 2σ to 3σ are *1* to *4*, so that the influence of noise decreases. Hence reference value *R* is preferably *4* to *8*, which can be obtained by adding *3* to *4* to these values in the same way as above.

Depending on the degree of influence of noise, there is a danger that the signal itself may end up being treated as noise. The method of comparing the difference of the average pixel value of both fields with reference value

R is effective in this sense, as it reduces the influence of noise.

(Second Embodiment)

FIG. 12 shows a construction of an image signal processing circuit that is the second embodiment of the invention. In the first embodiment, intra-field interpolation is automatically performed when output α of the difference judgement circuit is *1*. This being so, flicker or unnaturalness may be seen in the resulting image at the point where inter-field interpolation was switched to intra-field interpolation. To overcome this problem, the image signal processing circuit of the second embodiment generates a weighting factor based on output α of the difference judgement circuit, and weights and adds together intra-field interpolation and inter-field interpolation. In this way, the change between inter-field interpolation and intra-field interpolation becomes blurry, with it being possible to prevent the unnaturalness of the image.

In FIG. 12, the field memories 1 and 2, the interpolation circuit 3, a difference judgement circuit 15, the double-speed conversion memories 6 and 7, and the selection circuit 8 have the same constructions as those shown in FIG. 1, so that their explanation has been omitted.

An intermediate value selection circuit 14, unlike the intermediate value selection circuit 4 in FIG. 1, does not receive output α of the difference judgement circuit 15. In other words, the intermediate value selection circuit 14 has the same construction as the conventional circuit shown in FIG. 19.

A specific example of this circuit is shown in FIG. 13.

Apart from these circuits, the image signal processing circuit of this embodiment further includes a weighting factor setting circuit 11, a weighting/addition circuit 12, and an interpolation circuit 9.

The weighting factor setting circuit 11 calculates weighting factor β, based on comparison result α of the difference judgement circuit 15. The following two methods can be used to determine β.

The first method is as follows. The weighting factor setting circuit 11 operates a spatial low-pass filter (hereafter "LPF") for comparison result α of the difference judgement circuit 15. As an example, when a pixel to be interpolated is a pixel shown by a diagonally shaded broken-line circle in FIG. 14, the spatial LPF is operated in a range enclosed by a broken-line box.

Since broken-line pixels other than the diagonally

shaded one are also pixels which are subjected to interpolation, α is calculated for each of these pixels, with the calculated values of α being set as $\alpha 00$ to $\alpha 22$. This being so, β is calculated as

$$\beta = ((\alpha 00+\alpha 20+\alpha 02+\alpha 22) +2\times(\alpha 10+\alpha 01+\alpha 21+\alpha 12)+4\times\alpha 11)/4$$

The same calculation is used to find β, in the case where the coefficient of the LPF or the range for which the LPF operates is varied. This method enables the value of α for each pixel to change smoothly. As a result, the change between inter-field interpolation and intra-field interpolation becomes not so distinct, thereby producing a natural-looking image.

The second method is as follows. Here, output α of the difference judgement circuit 15 is not set at 0 or 1. Instead, $\Delta L-D$ is computed where ΔL is the difference between pixel value PB of the $(n-1)$th field and pixel value SB of the $(n+1)$th field and D is another predetermined value. If $\Delta L-D \leq 0$, $\alpha=0$ is output. If $\Delta L-D>0$, $\alpha=\Delta L-D$ is output. The weighting factor setting circuit 11 has predetermined value Z. The weighting factor setting circuit 11 determines β in the following manner, with Z being a predetermined value. When $\alpha=0$, $\beta=0$. When $\alpha \geq Z$,

$\beta=1$. When $0<\alpha<Z$, β is set within a range of 0 to 1 such that the inequality will not change before and after the conversion from α to β. According to this method, the inter-frame difference for each pixel directly affects the value of β, so that inter-field interpolation and intra-field interpolation are switched appropriately. This enables an image of high resolution to be obtained.

The interpolation circuit 9 generates an interpolation signal from pixels of the nth field, using the image signal output from the field memory 1. The interpolation circuit 9 has the same construction as the interpolation circuit 3. In some cases, it is possible to omit the interpolation circuit 9 and apply the output of the interpolation circuit 3 to the weighting/addition circuit 12.

The weighting/addition circuit 12 receives interpolation pixel value IN from the intermediate value selection circuit 14, interpolation signal R from the interpolation circuit 9, and weighting factor β from the weighting factor setting circuit 11. The weighting/addition circuit 11 calculates

$$Y=R\times\beta+IN\times(1-\beta)$$

and outputs Y as the final interpolation pixel value.

The double-speed conversion memory 6 sequentially stores interpolation pixel values *Y* output from the weighting/addition circuit 12. The double-speed conversion memory 7 sequentially stores pixel values *N* of image signals output from the field memory 1. The selection circuit 8 alternately reads interpolation pixel values *Y* from the double-speed conversion memory 6 and pixel values *N* from the double-speed conversion memory 7 and outputs them to the output terminal 20, in a period half the pixel period of the image signal input in the input terminal 10. In this way, a progressive scanned image signal is obtained in the output terminal 20.

According to the above construction, the final interpolation pixel value is generated by weighting and adding together the interpolation pixel value generated by the conventional intermediate value selection circuit and the intra-field interpolation value, based on the inter-frame difference. This suppresses the occurrence of conversion noise caused by the use of inter-field interpolation for a scene with large movement. Also, the change between intra-field interpolation and inter-field interpolation for each pixel becomes blur, by continuously changing the weighting factor in accordance with the judgement result of the difference judgement circuit. As a result, a favorable progressive scan

conversion result can be attained.

(Third Embodiment)

FIG. 15 shows an image signal processing circuit that is the third embodiment of the invention. The construction of this image signal processing circuit is basically the same as that of the first embodiment, except for the following. The image signal processing circuit of this embodiment is equipped with an edge detection circuit 131 for the image of the $(n-1)$th field and an edge detection circuit 132 for the image of the $(n+1)$th field. When any of the edge detection circuits 131 and 132 detects an edge, a gate of a gate circuit G is closed and judgement result α of the difference judgement circuit 5 is set at 0. As shown in FIG. 16, the edge detection circuit 131 detects whether an edge that extends in the horizontal direction is present between the pixel row of the mth line and the pixel row of the $(m-1)$th or $(m+1)$th line in the $(n-1)$th field. Likewise, the edge detection circuit 132 detects whether an edge extending in the horizontal direction is present between the mth line and the $(m-1)$th or $(m+1)$th line in the $(n+1)$th field. The detection may be performed using a known edge detection technique. This embodiment employs the following technique as one example. In FIG. 16, the difference in value of any two

vertically adjacent pixels between the pixel row of the *m*th line and the pixel row of the *(m-1)*th line is calculated. If the calculated differences have the same sign, an edge is judged as being present.

When an edge exists in any of the fields, difference judgement result α is set to *0*. In this way, images such as the following can be interpolated favorably.

FIG. 17 shows an image in which a black-colored horizontal line with luminance of *0* is placed in the center against the white-colored background. Suppose this image is moving downward. The moving speed is very slow, so that a gray-colored image is present at the same line (*m*th line) with the lines below being white even in the *(n+1)*th field, as shown in FIG. 18. When the construction of the first embodiment (see FIG. 1) is used in such a case, $\alpha=1$ since $|PB-SB|=|0-32|=32>7$ (reference value *R*), so that intra-field interpolation is performed. The resulting interpolation value is *255+240/2=147.5*, which is expressed by a light gray-colored line. However, when the image transition of the preceding and following fields is considered, this interpolation is clearly not desirable. On the other hand, if the conventional interpolation technique is used, the pixel of the *(n+1)*th field is set as the intermediate value, so that a blackish line is produced. Thus, the conventional interpolation

is preferable in this case. Accordingly, to interpolate an image that has a horizontally-extending edge, the conventional technique should be adopted instead of the method of the first embodiment. For this reason, if a horizontally-extending edge is detected, difference judgement result α is automatically set to 0 so as to execute the conventional interpolation, in the third embodiment.

The present invention is not limited to the above described constructions. Various modifications are possible so long as they do not depart from the scope of the invention. Example modifications are listed below.

(1) When the difference judgement circuit calculates an inter-frame difference, in each of the $(n-1)$th and $(n+1)$th fields the average value of a pixel group made up of pixel *PB* or *SB* corresponding to the pixel in the nth field to be interpolated and neighboring pixels thereof may be calculated, with the difference between the two averages being set as the inter-frame difference. In so doing, the influence of noise of the input image signal upon the judgement result is reduced, with it being possible to improve the quality of the converted image.

(2) In the above embodiments, the inter-frame difference is calculated as the difference in value of pixels *PB* and *SB* in the $(n-1)$th and $(n+1)$th fields that

correspond to the pixel in the *n*th field which is to be interpolated. However, the inter-frame difference may be calculated as the difference between pixel values *PB* and *SB* in the *(n-3)*th and *(n+3)*th fields or as the difference between pixel value *PB* and *SB* in the *(n-5)*th and *(n+5)*th fields. In other words, pixels of any two fields can be used as long as the change of the image is detected. A method of taking a difference using two or more preceding fields and two or more following fields is also applicable, such as by calculating the difference between the weighted average of the corresponding pixels in the *(n-1)*th, *(n-3)*th, and *(n-5)*th fields and the weighted average of the corresponding pixels in the *(n+1)*th, *(n+3)*th, and *(n+5)*th fields.

(3) The inter-frame difference is described as being calculated in absolute value in the above embodiments, but it may be calculated with a sign, where $PB>SB$ and $PB<SB$ are discriminated. In such a case, two reference values are set so that, for example, the reference value in the case of $PB>SB$ is larger than the reference value in the case of $PB<SB$, or smaller than the reference value in the case of $PB<SB$. Such assigning hysteresis to the reference values enables interpolation to be carried out more flexibly.

INDUSTRIAL APPLICABILITY

The present invention can be used to convert an interlaced image signal to a progressive scanned image signal while suppressing the occurrence of noise even when the image is a moving image. Hence the conventional problem of jaggies is reduced in the resulting progressive scanned image.

CLAIMS

1. An image signal processing apparatus for converting an image signal of a first scanning format to an image signal of a second scanning format, comprising:

main interpolating means for interpolating a scanning line between any two adjacent scanning lines in a present field that corresponds to the image signal of the first scanning format, by selectively executing two interpolation methods for each target pixel which constitutes the scanning line to be interpolated, the two interpolation methods being inter-field interpolation that uses pixels of a field preceding the present field and a field following the present field, and intra-field interpolation that uses pixels in the present field which are in a neighborhood of the target pixel;

change detecting means for detecting a change of an image, by referring to an image signal of the preceding field and an image signal of the following field;

automatic interpolating means for prohibiting, depending on a detection result obtained by the change detecting means, the main interpolating means to select and execute one of the two interpolation methods, and instead automatically executing a specific interpolation method; and

image signal outputting means for alternately outputting scanning lines of the image signal of the present field and interpolated scanning lines obtained by the combination of the main interpolating means, the change detecting means, and the automatic interpolating means.

2. The image signal processing apparatus of Claim 1,

wherein the change detecting means detects an extent to which the image changes with time, and

the automatic interpolating means automatically executes the intra-field interpolation, when the detected extent is greater than a reference value.

3. The image signal processing apparatus of Claim 2,

wherein the first scanning format is interlace scanning, and the second scanning format is progressive scanning, and

the image signal outputting means outputs a progressive scanned image signal of one frame, responsive to an interlaced image signal of one field.

4. The image signal processing apparatus of Claim

3,

wherein the change detecting means calculates a difference between a value of a pixel in the preceding field that positionally corresponds to the target pixel and a value of a pixel in the following field that positionally corresponds to the target pixel, and judges whether the difference is greater than the reference value.

5. The image signal processing apparatus of Claim 4,

wherein when the present field is an *n*th field, the preceding field is an *(n-1)*th field and the following field is an *(n+1)*th field,

the main interpolating means is equipped with a series circuit of at least two field memories, and

when the image signal of the *(n+1)*th field is being input in a field memory of a first stage in the series circuit, the image signal of the *n*th field is being output from the field memory of the first stage and the image signal of the *(n-1)*th field is being output from a field memory of a second stage in the series circuit.

6. The image signal processing apparatus of Claim 5,

wherein the main interpolating means includes:

an intermediate value selecting unit for selecting an intermediate value from (a) the value of the pixel in the *(n-1)*th field that positionally corresponds to the target pixel, (b) the value of the pixel in the *(n+1)*th field that positionally corresponds to the target pixel, and (c) an average value of pixels in the *n*th field that are adjacent to the target pixel, the intermediate value being smaller than one of remaining two values but greater than a different one of the remaining two values;

a first inter-field interpolating unit for obtaining high-frequency components from values of pixels in the *(n-1)*th field that are made up of the pixel positionally corresponding to the target pixel and neighboring pixels thereof, and calculating a first interpolation value for the target pixel using the high-frequency components;

a second inter-field interpolating unit for obtaining high-frequency components from values of pixels in the *(n+1)*th field that are made up of the pixel positionally corresponding to the target pixel and neighboring pixels thereof, and calculating a second interpolation value for the target pixel using the high-frequency components;

an intra-field interpolating unit for calculating a third interpolation value for the target pixel, using

an average value of the pixels in the *n*th field that are in the neighborhood of the target pixel; and

a selecting unit for selecting one of the first inter-field interpolating unit, the second inter-field interpolating unit, and the intra-field interpolating unit based on the intermediate value selected by the intermediate value selecting unit, and outputting an interpolation value calculated by the selected interpolating unit to the image signal outputting means as a pixel value of the target pixel.

7. The image signal processing apparatus of Claim 4,

wherein the reference value is set at a value in a range of *7* to *16*, when the image is expressed in *256* levels of gray.

8. The image signal processing apparatus of Claim 3,

wherein the change detecting means calculates a difference between an average value of a pixel group in the preceding field and an average value of a pixel group in the following field, and judges whether the difference is greater than the reference value, each pixel group being made up of a pixel that positionally corresponds to the

target pixel and neighboring pixels thereof.

9. The image signal processing apparatus of Claim 4, further comprising:

edge detecting means for detecting an edge in the preceding field or the following field, the edge being parallel to a scanning line that includes a pixel positionally corresponding to the target pixel; and

stopping means for temporarily stopping the automatic interpolating means from prohibiting the main interpolating means, when the edge detecting means detects the edge.

10. An image signal processing apparatus for converting an image signal of a first scanning format to an image signal of a second scanning format, comprising:

main interpolating means for interpolating a scanning line between any two adjacent scanning lines in a present field that corresponds to the image signal of the first scanning format, by selectively executing inter-field interpolation and intra-field interpolation to calculate a first interpolation value for each target pixel which constitutes the scanning line to be interpolated, the inter-field interpolation using pixels of a field preceding the present field and a field

following the present field, and the intra-field interpolation using pixels in the present field that are in a neighborhood of the target pixel;

sub-interpolating means for executing the intra-field interpolation to calculate a second interpolation value for the target pixel, using the pixels in the present field that are in the neighborhood of the target pixel;

change detecting means for detecting a change of an image, by referring to an image signal of the preceding field and an image signal of the following field;

weight setting means for setting a first weight by which the first interpolation value should be multiplied, and a second weight by which the second interpolation value should be multiplied;

weighting/adding means for multiplying, depending on a detection result obtained by the change detecting means, the first interpolation value by the first weight and the second interpolation value by the second weight, and calculating a sum of the weighted first interpolation value and the weighted second interpolation value, the sum being set as a value of the target pixel; and

image signal outputting means for alternately outputting scanning lines of the image signal of the present field and interpolated scanning lines obtained by the combination of the main interpolating means, the

sub-interpolating means, the change detecting means, the weight setting means, and the weighting/adding means.

11. The image signal processing apparatus of Claim 10,

wherein the first scanning format is interlace scanning, and the second scanning format is progressive scanning, and

the image signal outputting means outputs a progressive scanned image signal of one frame, responsive to an interlaced image signal of one field.

12. The image signal processing apparatus of Claim 11,

wherein the change detecting means calculates a difference between a value of a pixel in the preceding field that positionally corresponds to the target pixel and a value of a pixel in the following field that positionally corresponds to the target pixel, and judges whether the difference is greater than the reference value.

13. The image signal processing apparatus of Claim 12,

wherein the weight setting means sets the first

weight and the second weight, in accordance with the difference obtained for the target pixel and differences obtained for pixels in the present field that are subjected to interpolation and are in a neighborhood of the target pixel.

14. The image signal processing apparatus of Claim 12,

wherein the weight setting means sets the first weight and the second weight, in accordance with the difference calculated by the change detecting means.

15. An image signal processing apparatus for interpolating necessary scanning lines, when converting an interlaced image signal to a progressive scanned image signal, comprising:

a first interpolating circuit for generating an interpolation value *M* for each target pixel which constitutes a scanning line to be interpolated in an *n*th field that corresponds to the interlaced image signal, by performing interpolation within the *n*th field;

an intermediate value selecting circuit for selecting an intermediate value from (a) a value *P* of a pixel in an *(n-1)*th field that positionally corresponds to the target pixel, (b) a value *S* of a pixel in an *(n+1)*th

field that positionally corresponds to the target pixel, and (c) the interpolation value M, the intermediate value being smaller than one of remaining two values but greater than a different one of the remaining two values;

a difference judging circuit for calculating a difference ΔL using an image signal of the $(n-1)$th field and an image signal of the $(n+1)$th field, and outputting a judgement result based on a comparison between the difference ΔL and a reference value R; and

a target pixel generating circuit for outputting, as a value of the target pixel, (a) the interpolation value M, when the difference judging circuit judges $\Delta L \geq R$ or the intermediate value selecting circuit selects the interpolation value M, (b) a first interpolation value for the target pixel which is generated by performing first inter-field interpolation that uses at least the image signal of the $(n-1)$th field, when the difference judging circuit judges $\Delta L < R$ and the intermediate value selecting circuit selects the value P, and (c) a second interpolation value for the target pixel which is generated by performing second inter-field interpolation that uses at least the image signal of the $(n+1)$th field, when the difference judging circuit judges $\Delta L < R$ and the intermediate value selecting circuit selects the value S.

16. The image signal processing apparatus of Claim 15,

wherein the target pixel generating circuit includes:

a first high-frequency component extracting circuit for extracting high-frequency components from pixels in the *(n-1)*th field which are consecutive in a vertical direction;

a second high-frequency component extracting circuit for extracting high-frequency components from pixels in the *(n+1)*th field which are consecutive in the vertical direction;

a second interpolating circuit for generating a third interpolation value for the target pixel, by performing interpolation within the *n*th field;

a first calculating circuit for performing a calculation, using the high-frequency components extracted by the first high-frequency component extracting circuit and the third interpolation value; and

a second calculating circuit for performing a calculation, using the high-frequency components extracted by the second high-frequency component extracting circuit and the third interpolation value, and

a result of the calculation by the first calculating circuit is the first interpolation value, whereas a result

of the calculation by the second calculating circuit is the second interpolation value.

17. An image signal processing apparatus for interpolating necessary scanning lines, when converting an interlaced image signal to a progressive scanned image signal, comprising:

a first interpolating circuit for generating an interpolation value *M* for each target pixel which constitutes a scanning line to be interpolated in an *n*th field that corresponds to the interlaced image signal, by performing interpolation within the *n*th field;

an intermediate value selecting circuit for selecting an intermediate value from (a) a value *P* of a pixel in an *(n-1)*th field that positionally corresponds to the target pixel, (b) a value *S* of a pixel in an *(n+1)*th field that positionally corresponds to the target pixel, and (c) the interpolation value *M*, the intermediate value being smaller than one of remaining two values but greater than a different one of the remaining two values;

a difference judging circuit for calculating a difference ΔL using an image signal of the *(n-1)*th field and an image signal of the *(n+1)*th field, and outputting a judgement result based on a comparison between the difference ΔL and a reference value *R*;

a first high-frequency component extracting circuit for extracting high-frequency components from pixels in the *(n-1)*th field which are consecutive in a vertical direction;

a second high-frequency component extracting unit for extracting high-frequency components from pixels in the *(n+1)*th field which are consecutive in the vertical direction;

a second interpolating circuit for generating a first interpolation value for the target pixel, by performing interpolation within the *n*th field;

a first calculating circuit for performing a calculation, using the high-frequency components extracted by the first high-frequency component extracting circuit and the first interpolation value;

a second calculating circuit for performing a calculation, using the high-frequency components extracted by the second high-frequency component extracting circuit and the first interpolation value;

a selecting circuit for selecting and outputting (a) the interpolation value *M*, when the intermediate value selecting circuit selects the interpolation value *M*, (b) a result of the calculation by the first calculating circuit, when the intermediate value selecting circuit selects the value *P*, and (c) a result of the calculation

by the second calculating circuit, when the intermediate value selecting circuit selects the value *S*;

a third interpolating circuit for generating a second interpolation value for the target pixel, by performing interpolation within the *n*th field;

a weight setting circuit for setting a first weight by which an output value of the selecting circuit should be multiplied and a second weight by which the second interpolation value should be multiplied, according to the judgement result by the difference judging circuit; and

a weighting/adding circuit for multiplying the output value of the selecting circuit by the first weight and the second interpolation value by the second weight, and outputting a sum of the weighted values as a value of the target pixel.

18. The image signal processing apparatus of Claim 17,

wherein the difference judging circuit calculates a difference between the value *P* and the value *S* as the difference ΔL, and outputs the judgement result based on the comparison between the difference ΔL and the reference value *R*.

19. The image signal processing apparatus of Claim 17,

wherein the difference judging circuit calculates a difference between an average value of a pixel group in the $(n-1)$th field and an average value of a pixel group in the $(n+1)$th field as the difference ΔL, and outputs the judgement result based on the comparison between the difference ΔL and the reference value R, each pixel group being made up of a pixel that positionally corresponds to the target pixel and neighboring pixels thereof.

20. The image signal processing apparatus of Claim 17,

wherein the difference judging circuit outputs 1 when $\Delta L \geq R$, and outputs 0 when $\Delta L < R$, and

the weight setting circuit calculates a value F, and sets the value F as the second weight and a value $(1-F)$ as the first weight, the value F being obtained by

(a) weighting output values of the difference judging circuit which correspond to pixels in a predetermined range in the nth field, according to a distance of each of the pixels from the target pixel, the pixels being made up of the target pixel and pixels which are subjected to interpolation and are in a neighborhood of the target pixel, and

(b) adding the weighted output values together.

21. The image signal processing circuit of Claim 17, wherein the difference judging circuit outputs a value G, G being a value in a range of 0 to 1 depending on a value $(R-\Delta L)$ when $\Delta L \geq R$, and being 0 when $\Delta L < R$, and the weight setting circuit sets the value G as the second weight, and a value $(1-G)$ as the first weight.

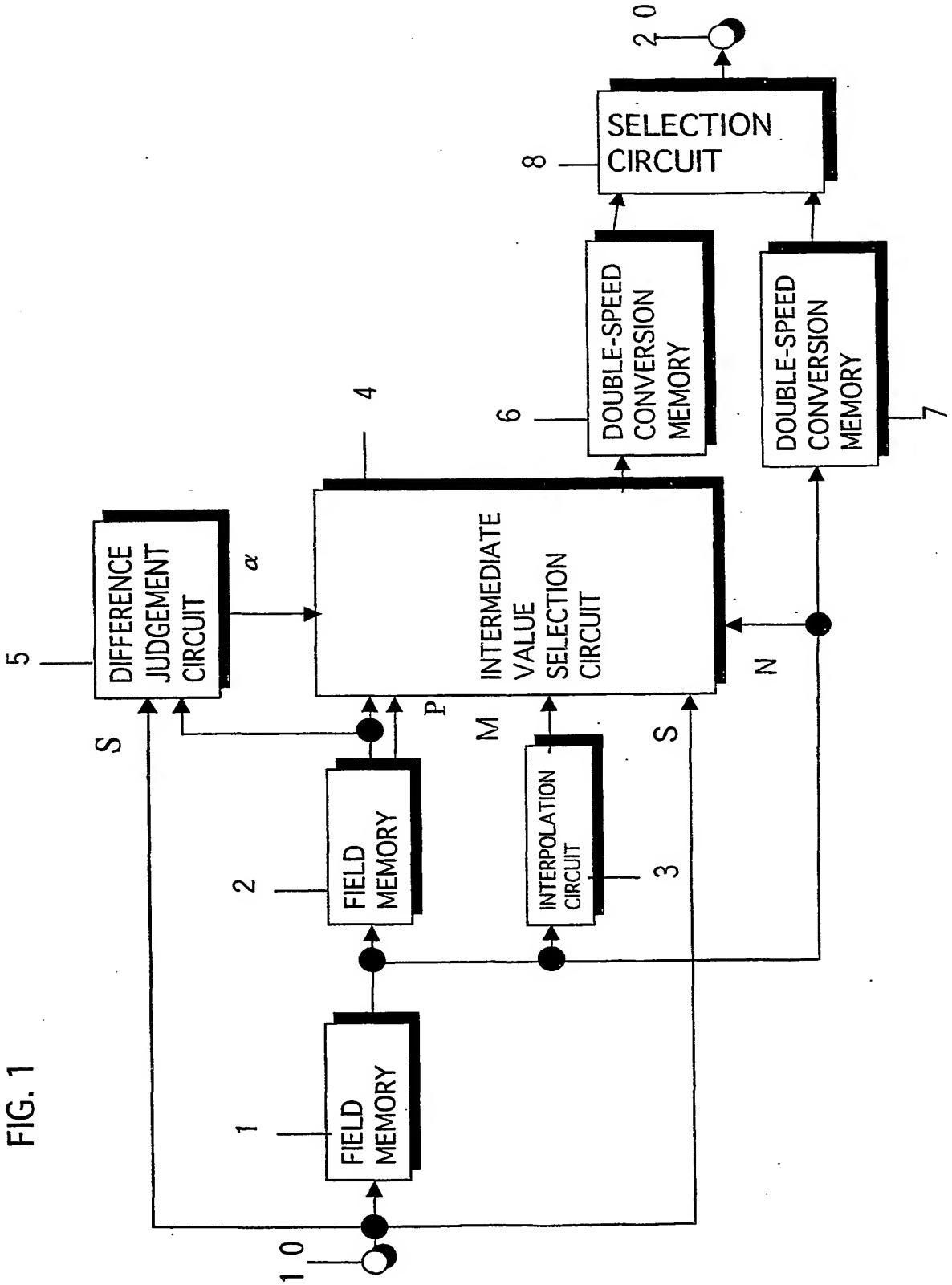
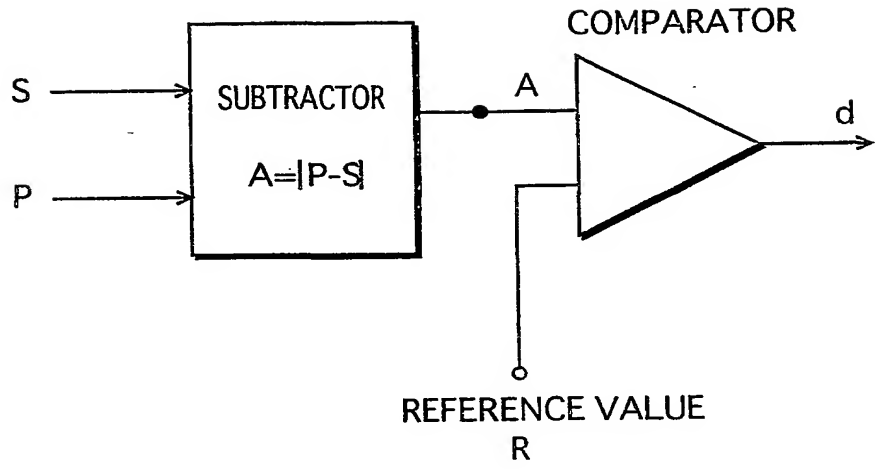


FIG. 1

FIG. 2



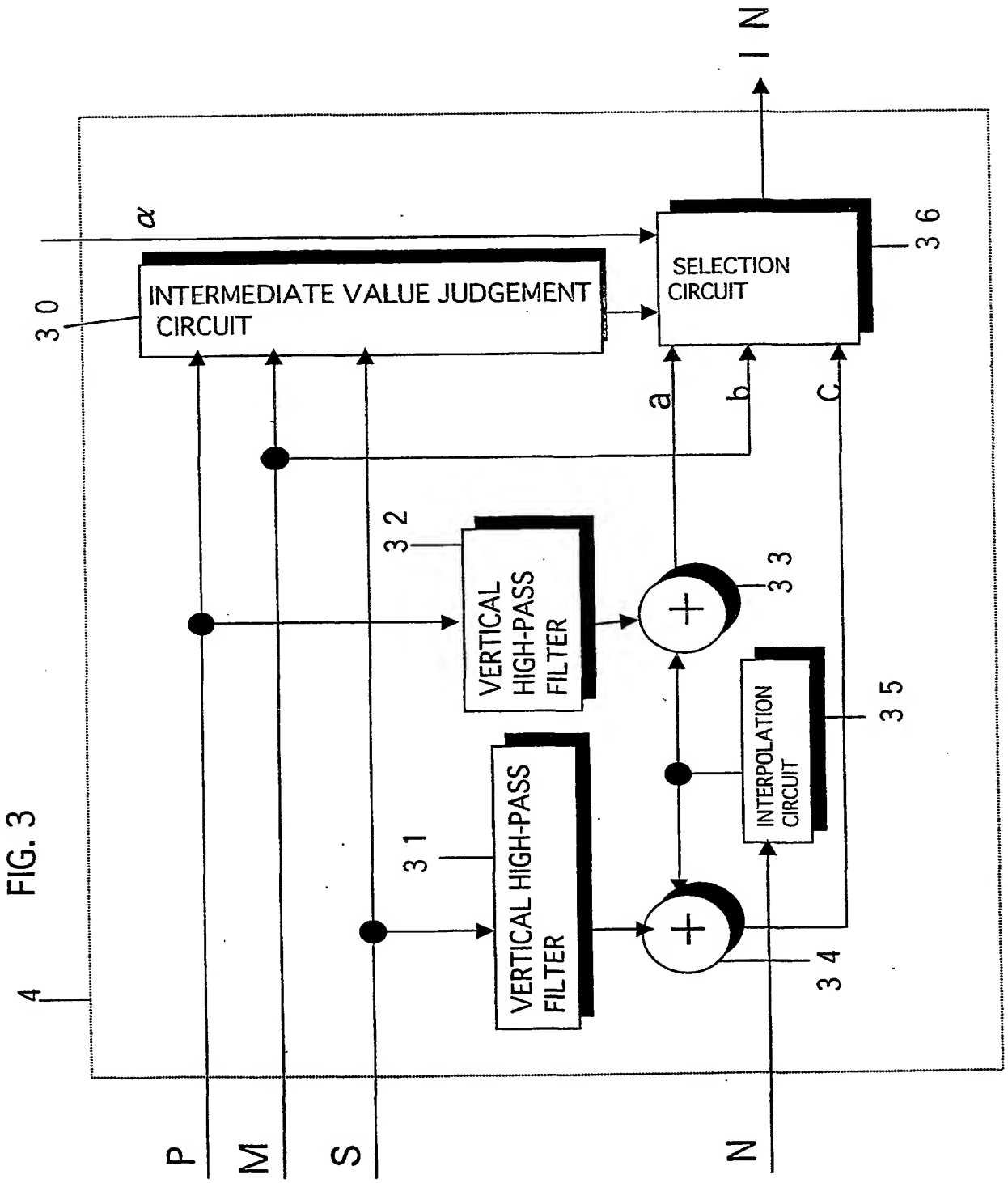


FIG. 3

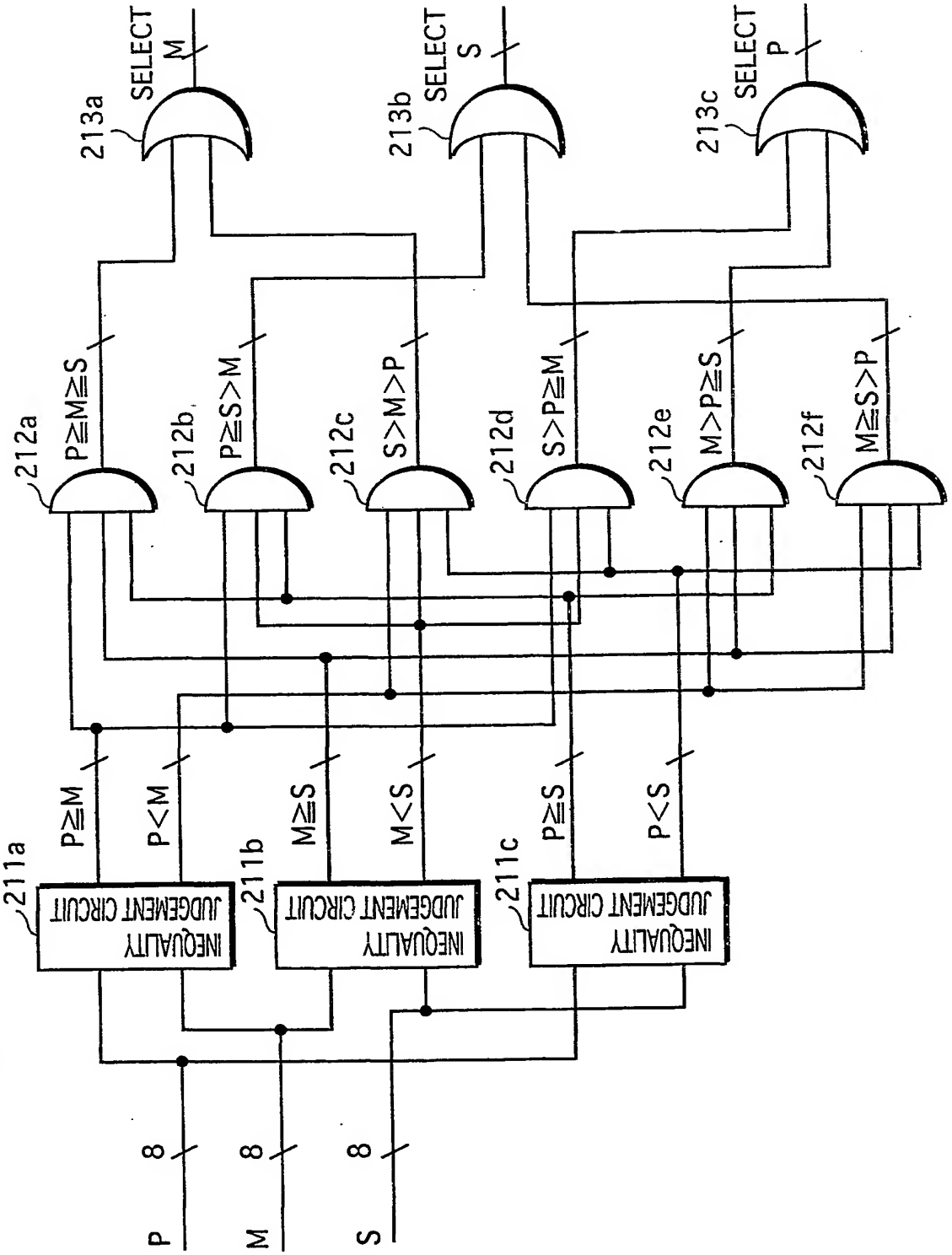


FIG. 4

FIG. 5

P>M	P>S	M>S	α	SELECT
1	0	0	0	a
0	1	1	0	a
1	1	1	0	b
0	0	0	0	b
1	1	0	0	c
0	0	1	0	c
*	*	*	1	b

*: 0 OR 1

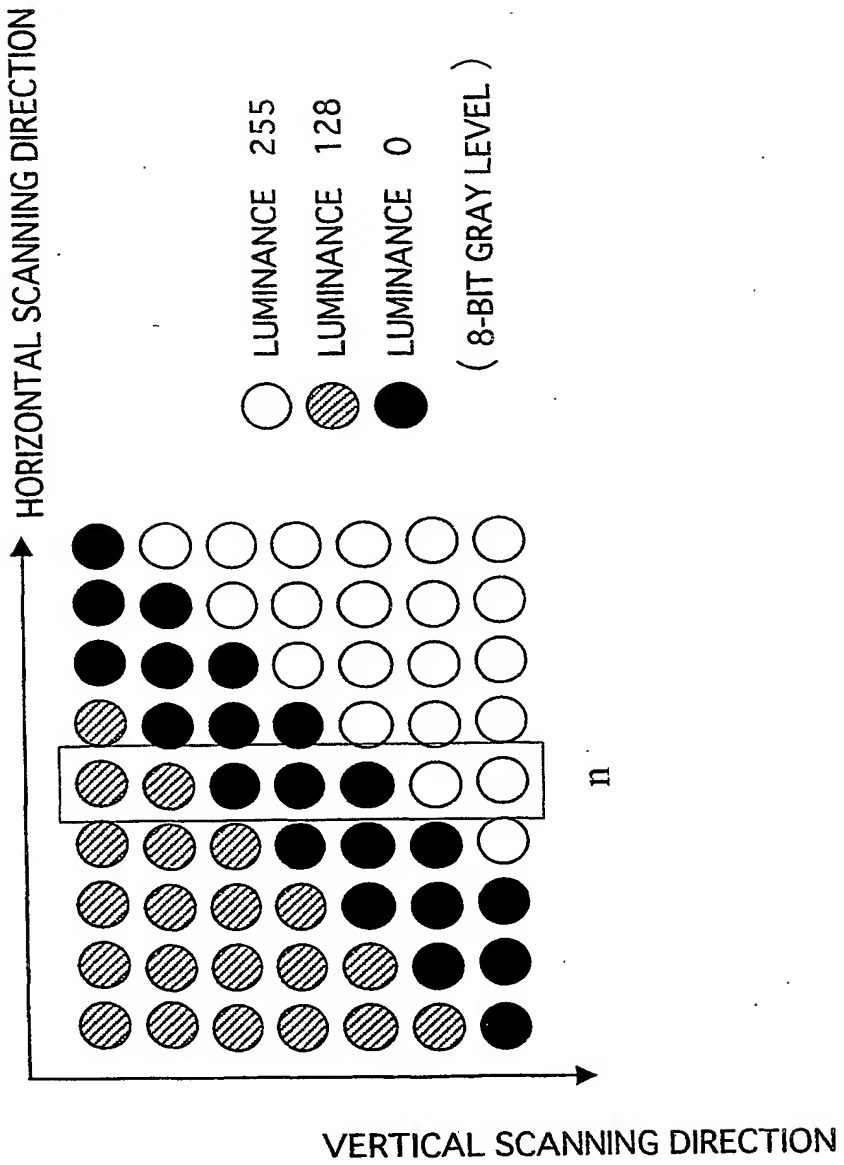
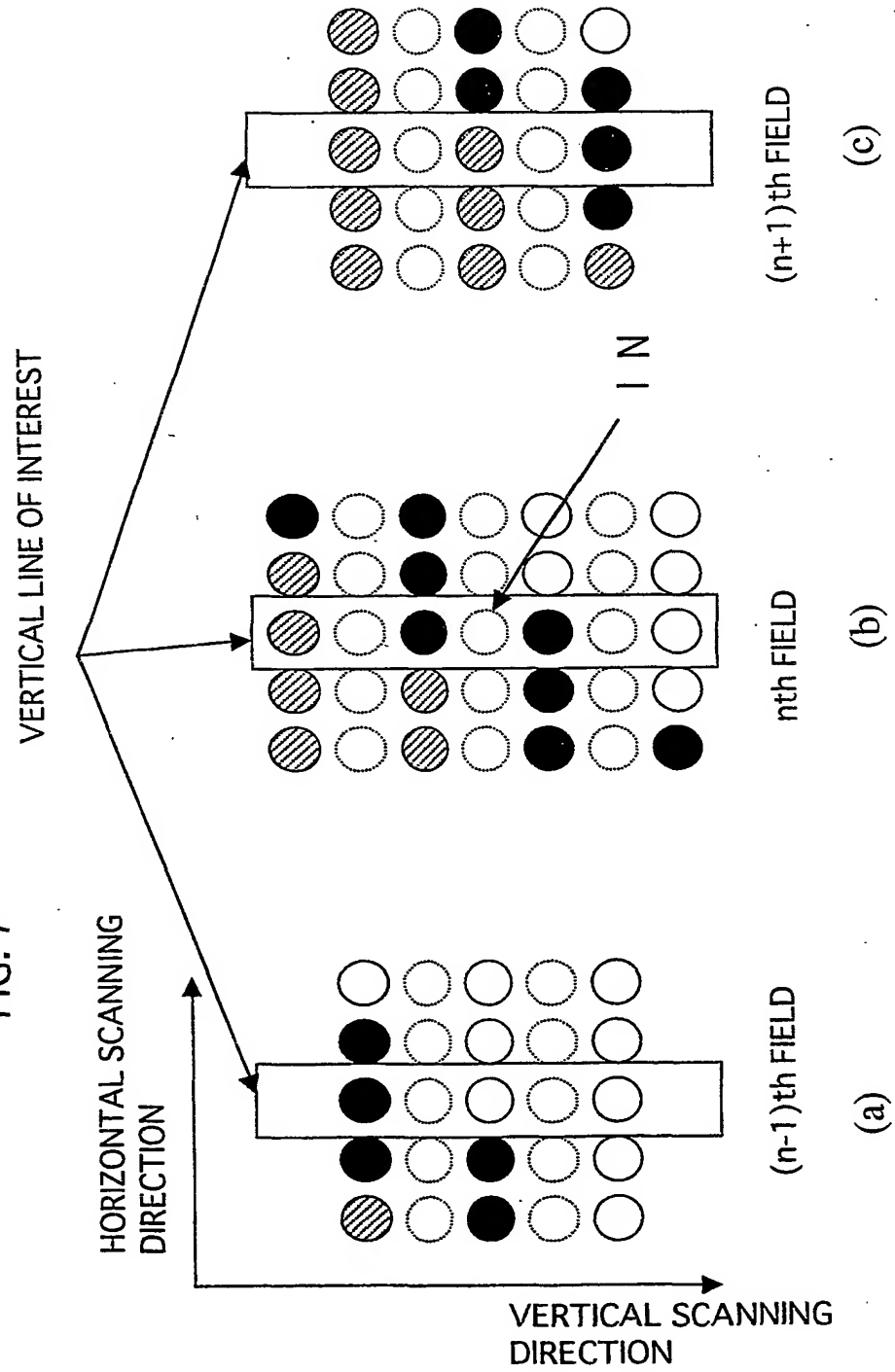


FIG. 6

FIG. 7



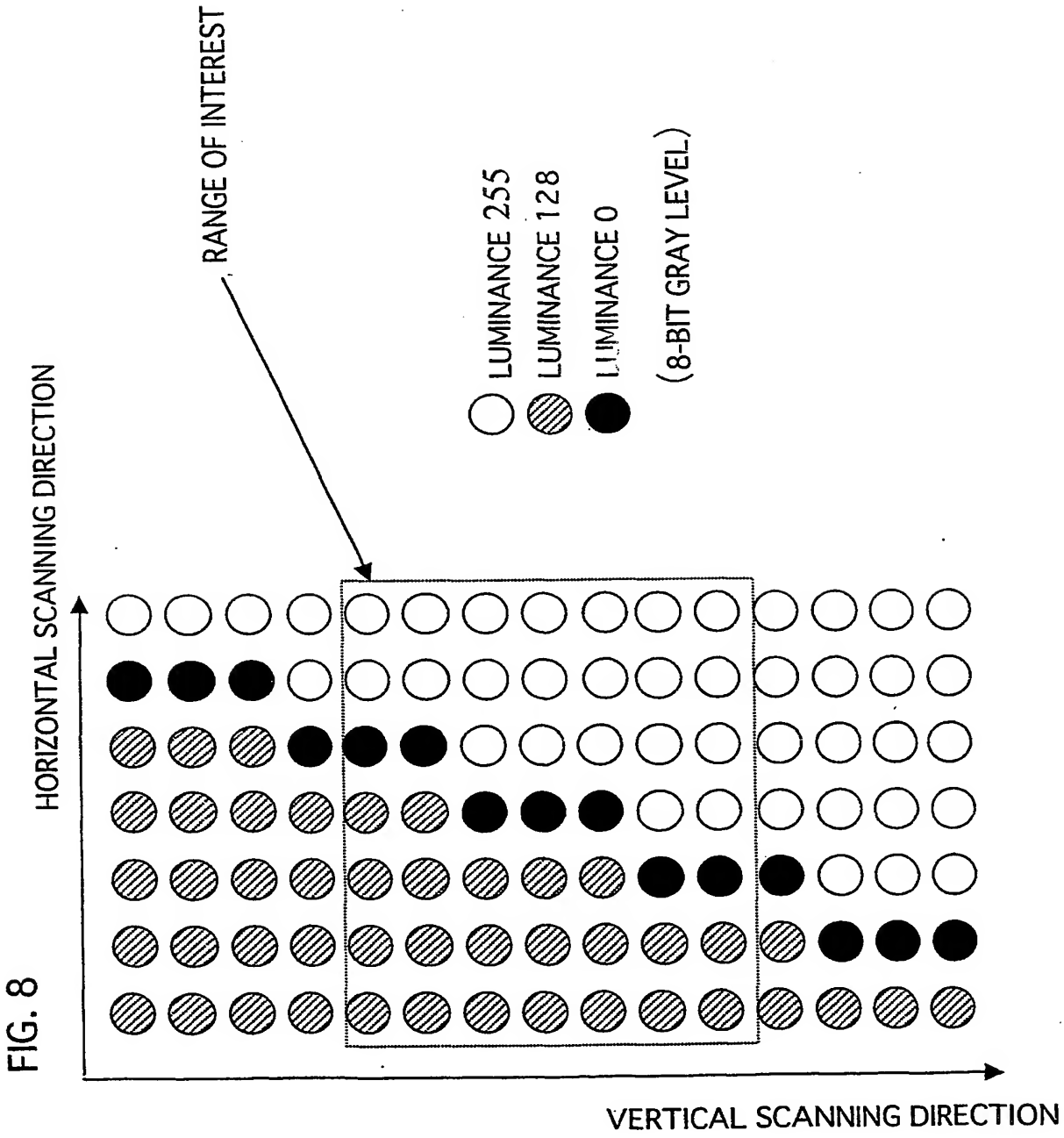
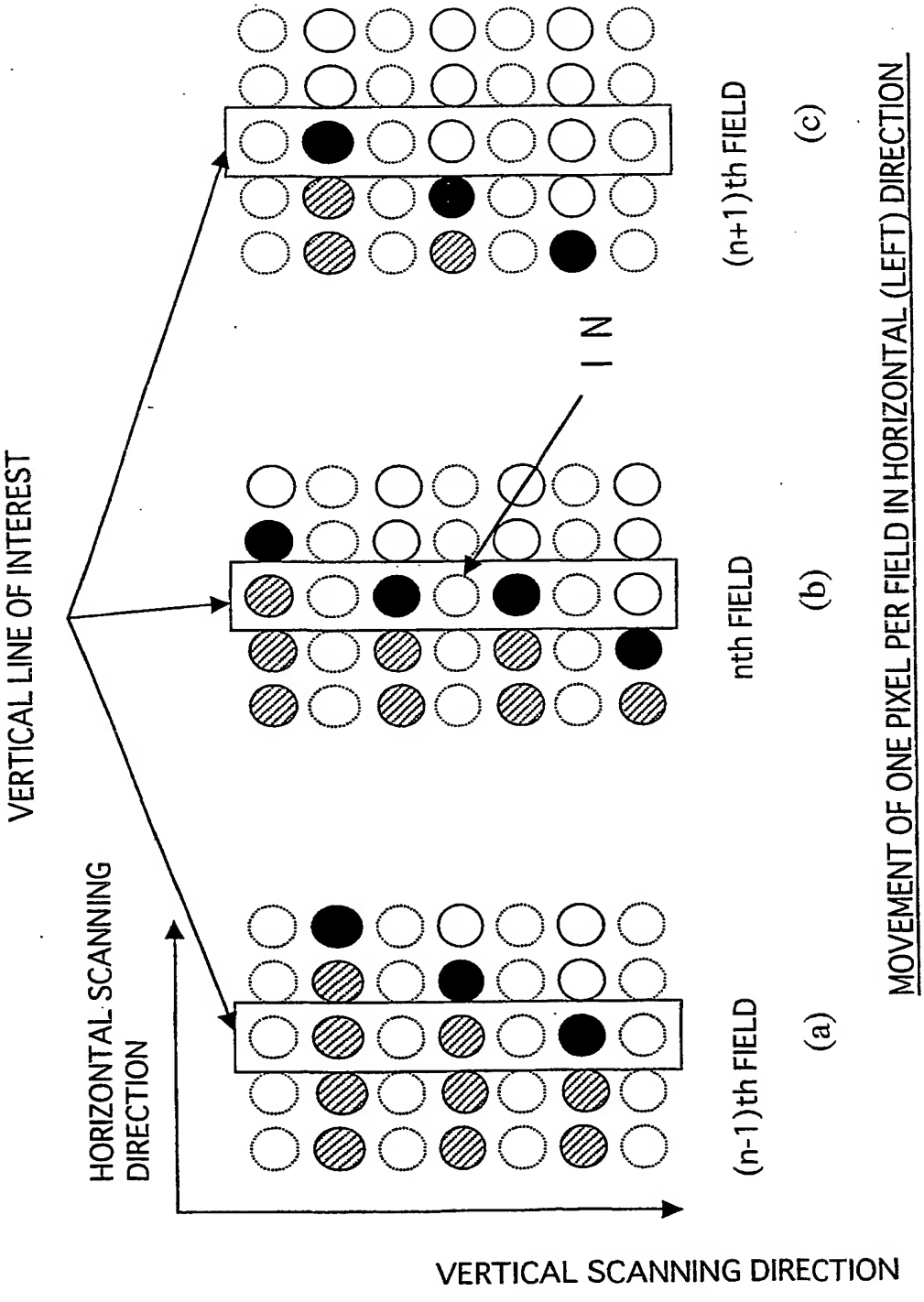


FIG. 8

FIG. 9



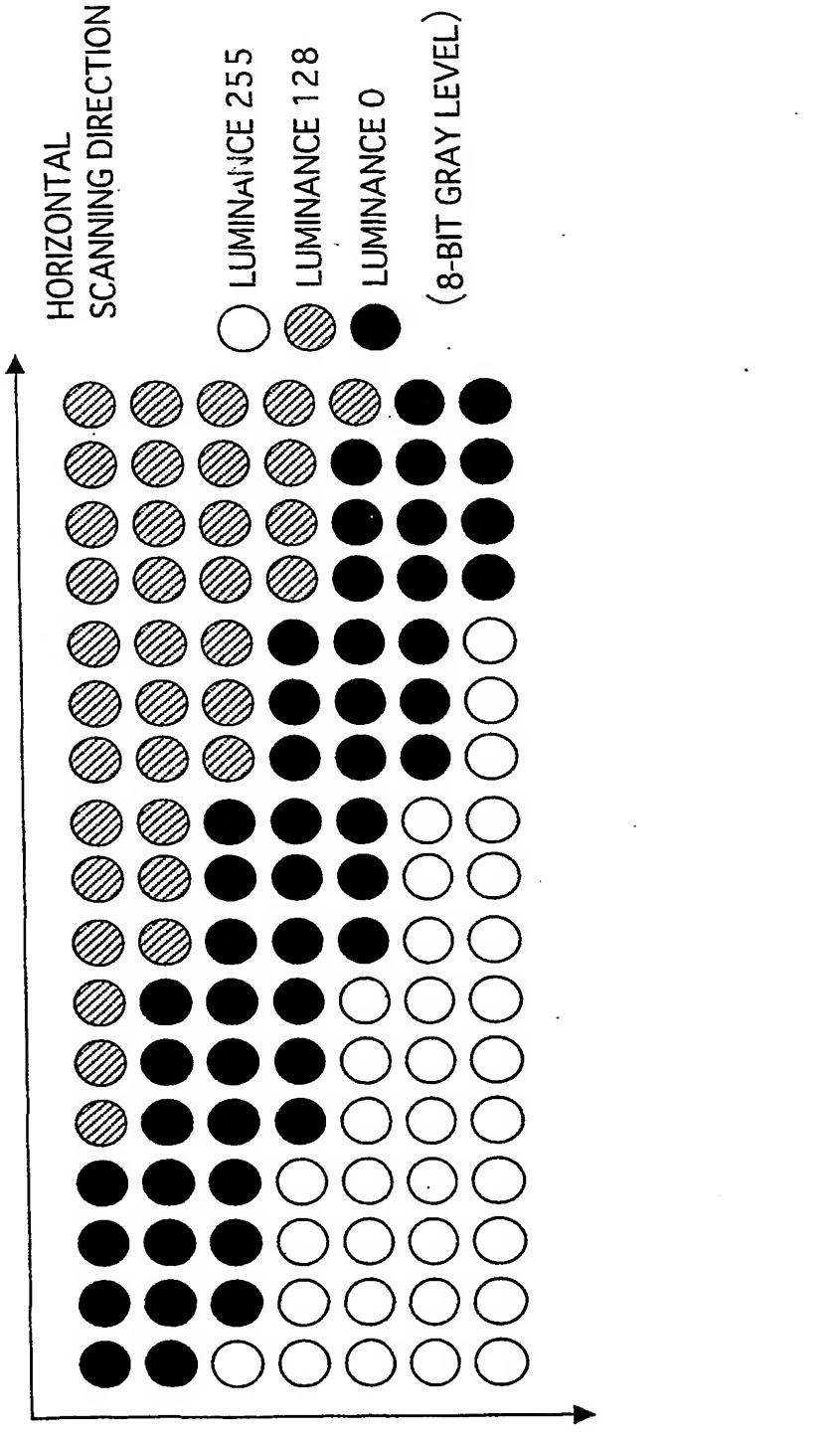
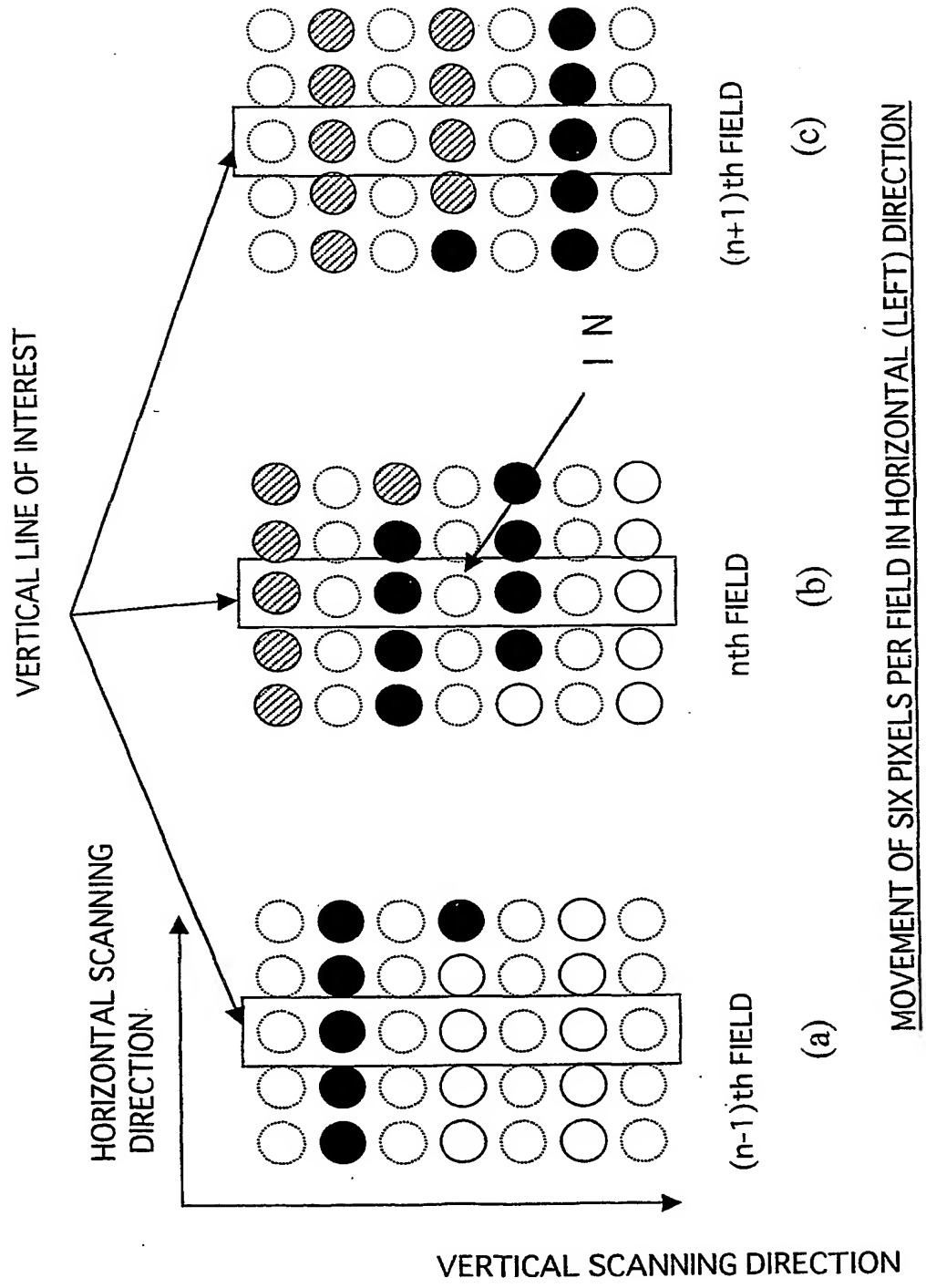


FIG. 10

FIG. 11



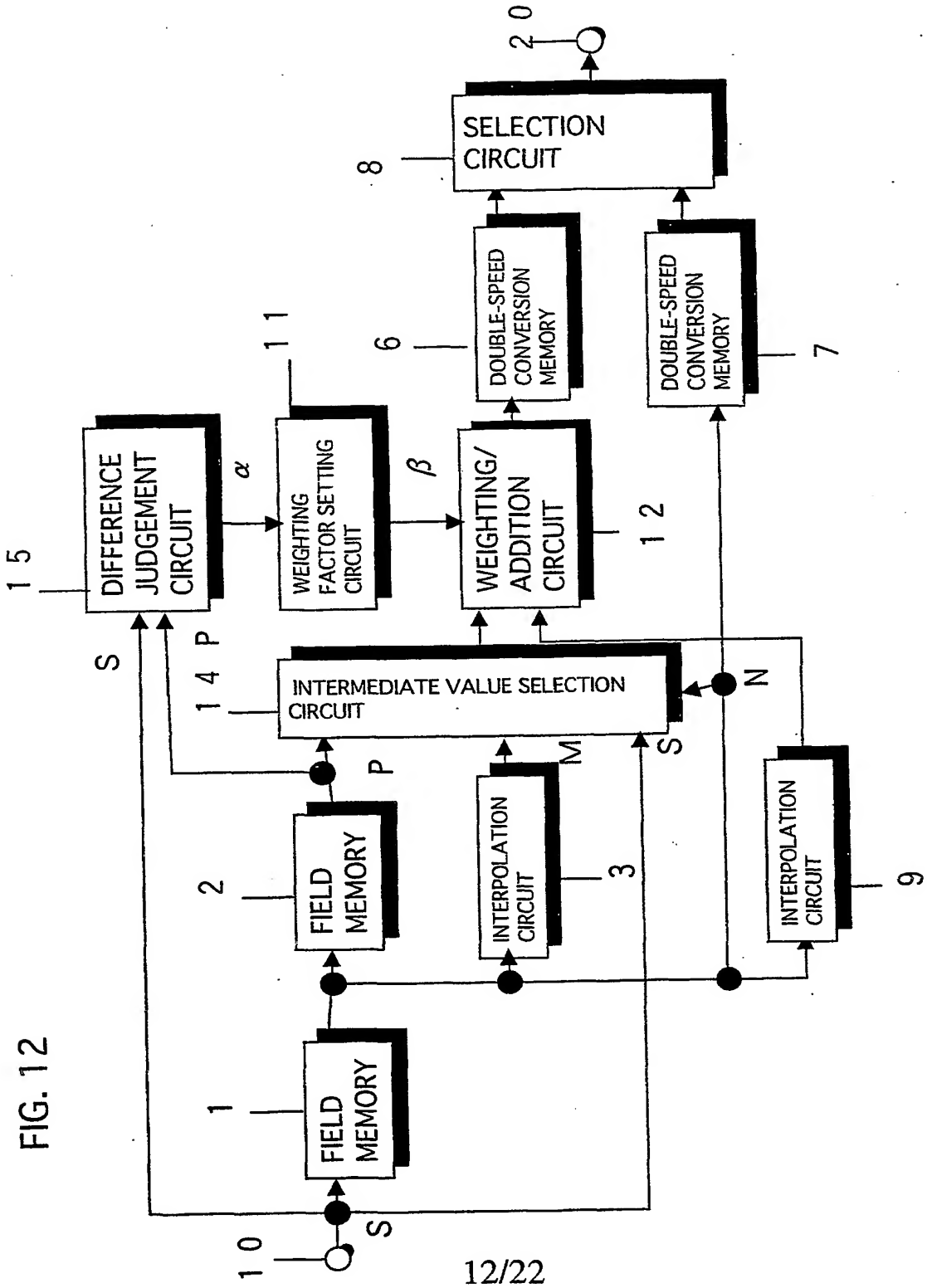


FIG. 12

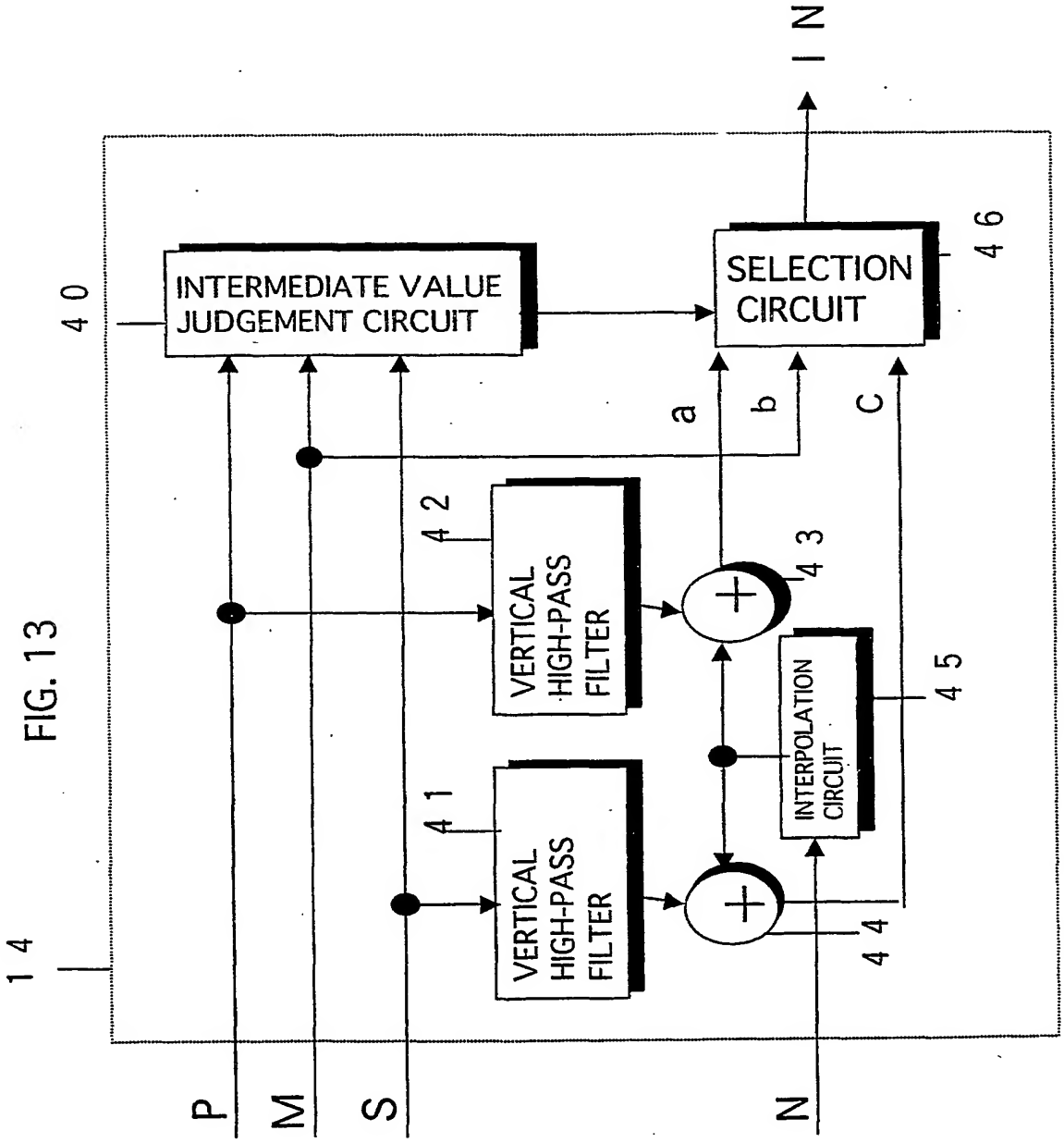


FIG. 13

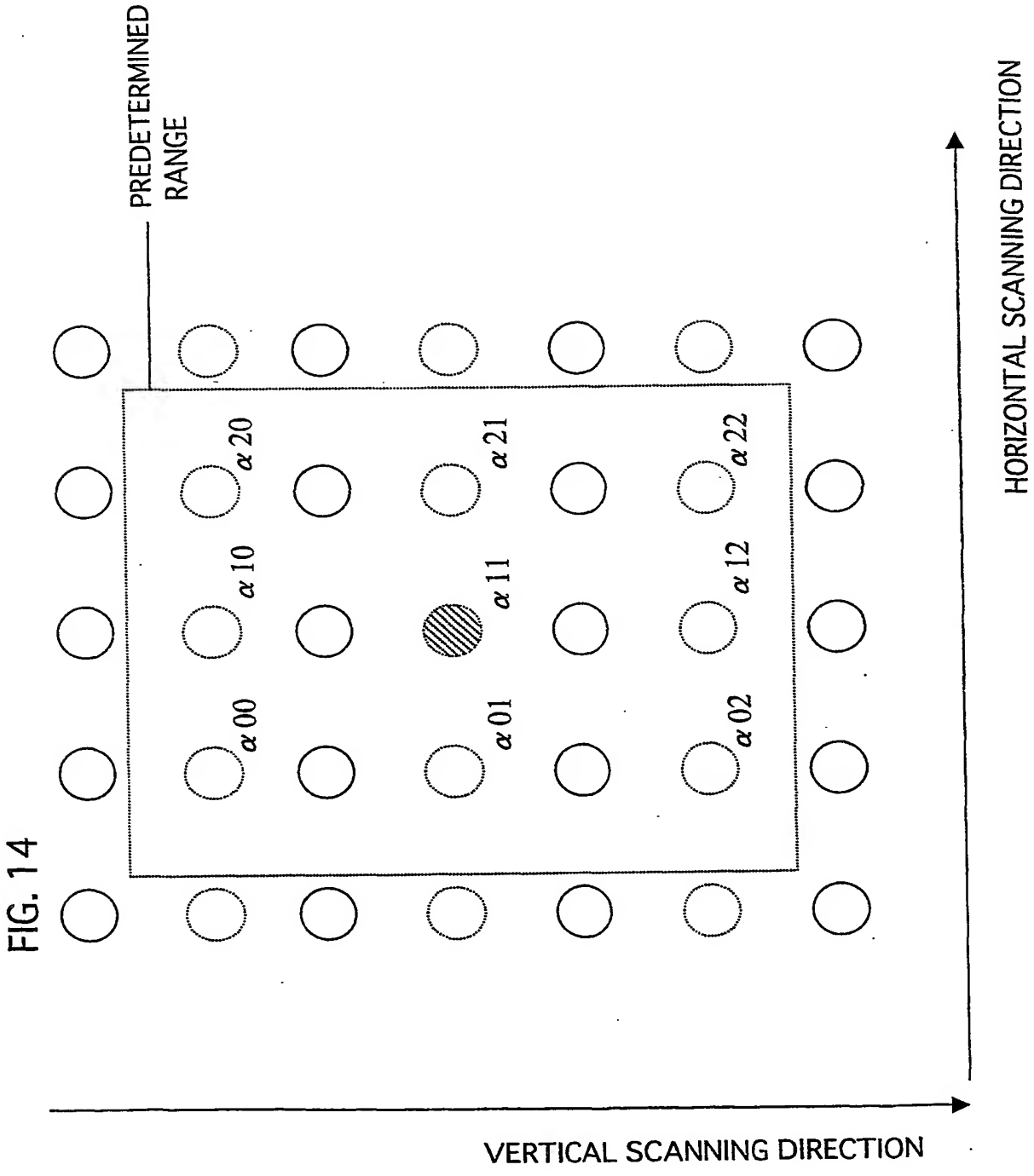


FIG. 14

FIG. 15

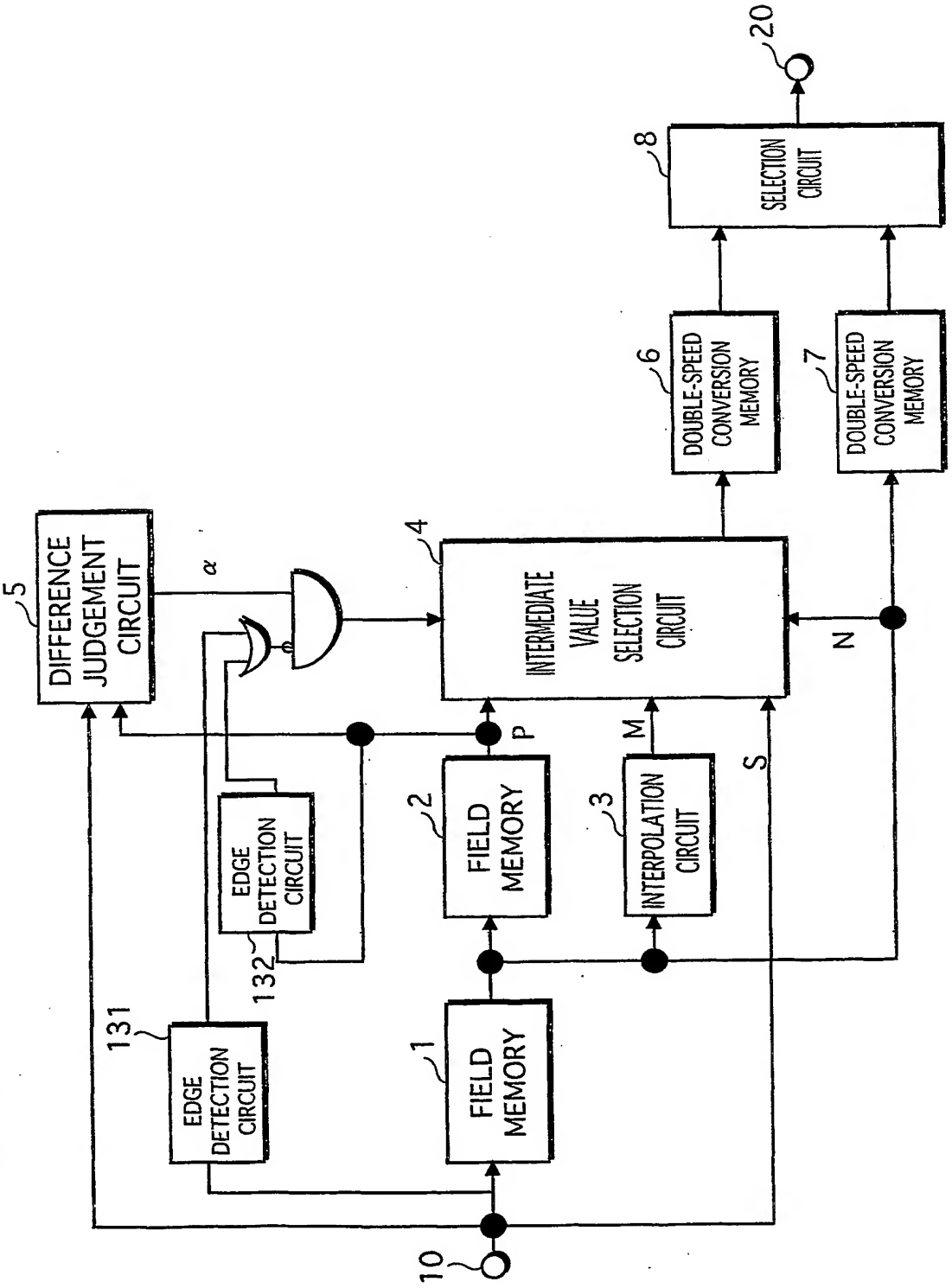
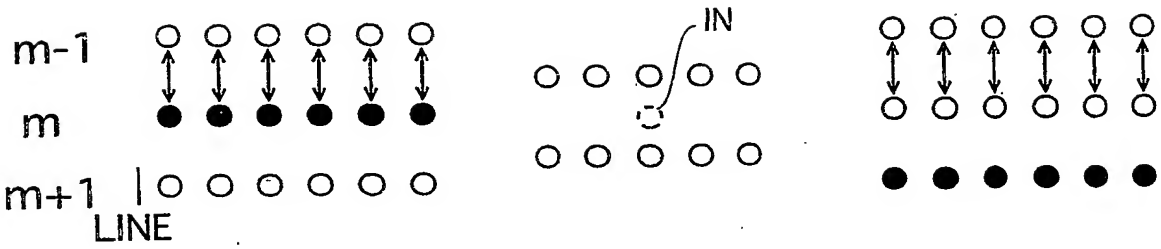


FIG. 16



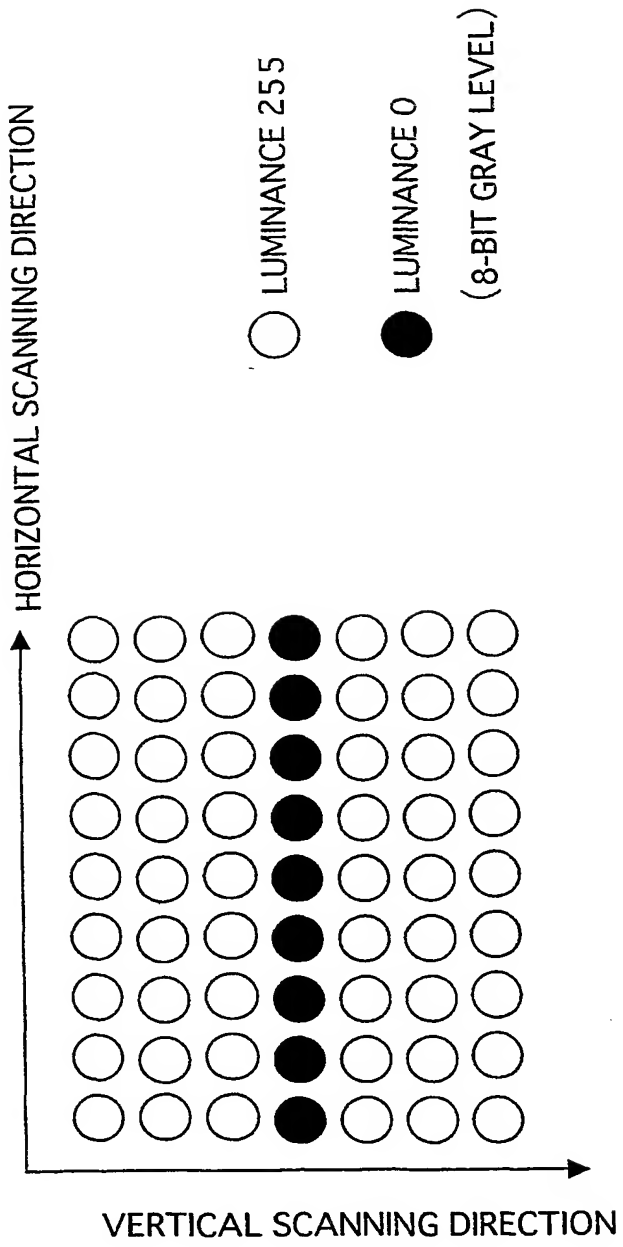


FIG. 17

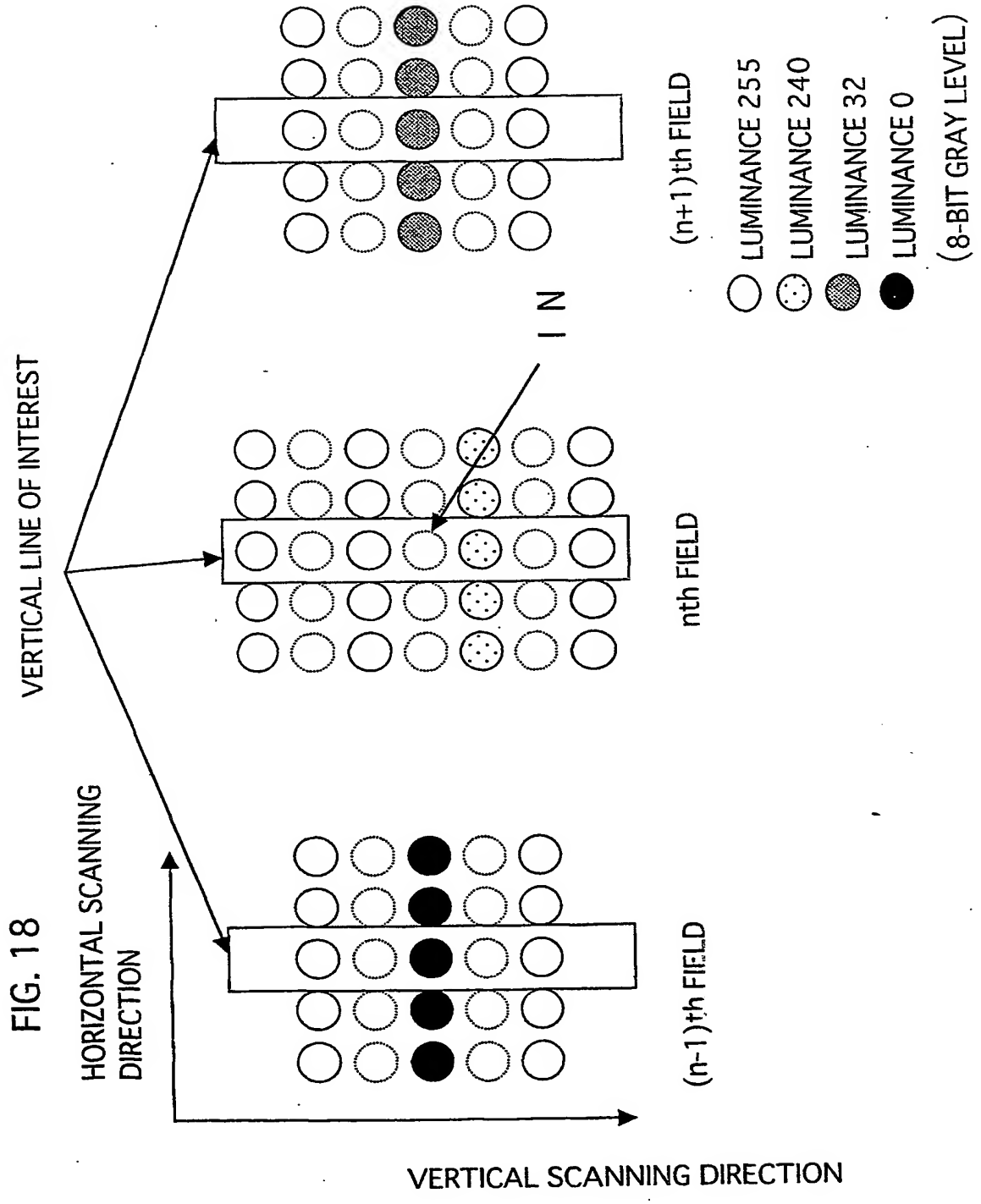


FIG. 18

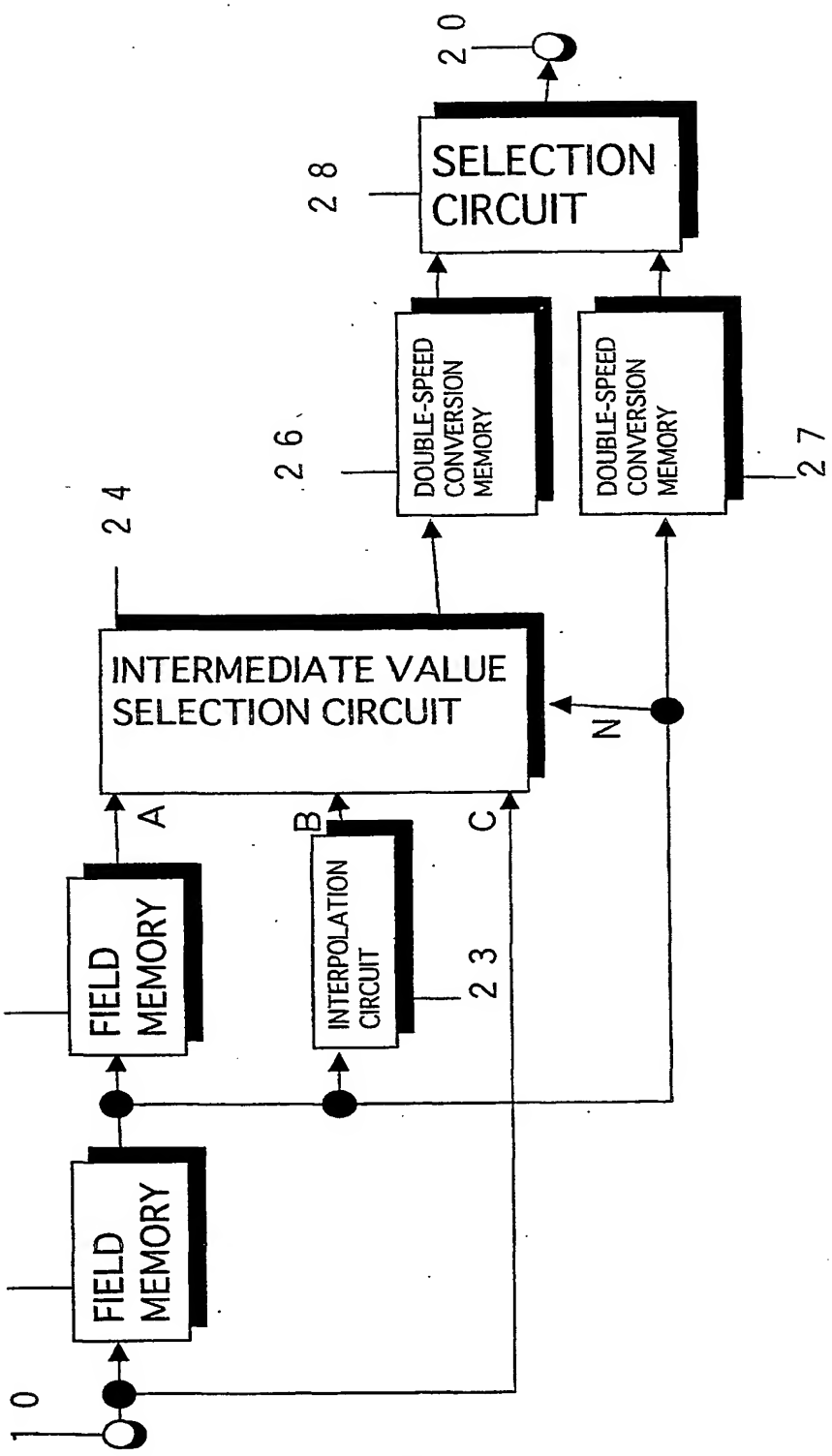


FIG. 19

FIG. 20

A>B	A>C	B>C	SELECT
1	0	0	A
0	1	1	A
1	1	1	B
0	0	0	B
1	1	0	C
0	0	1	C

FIG. 21

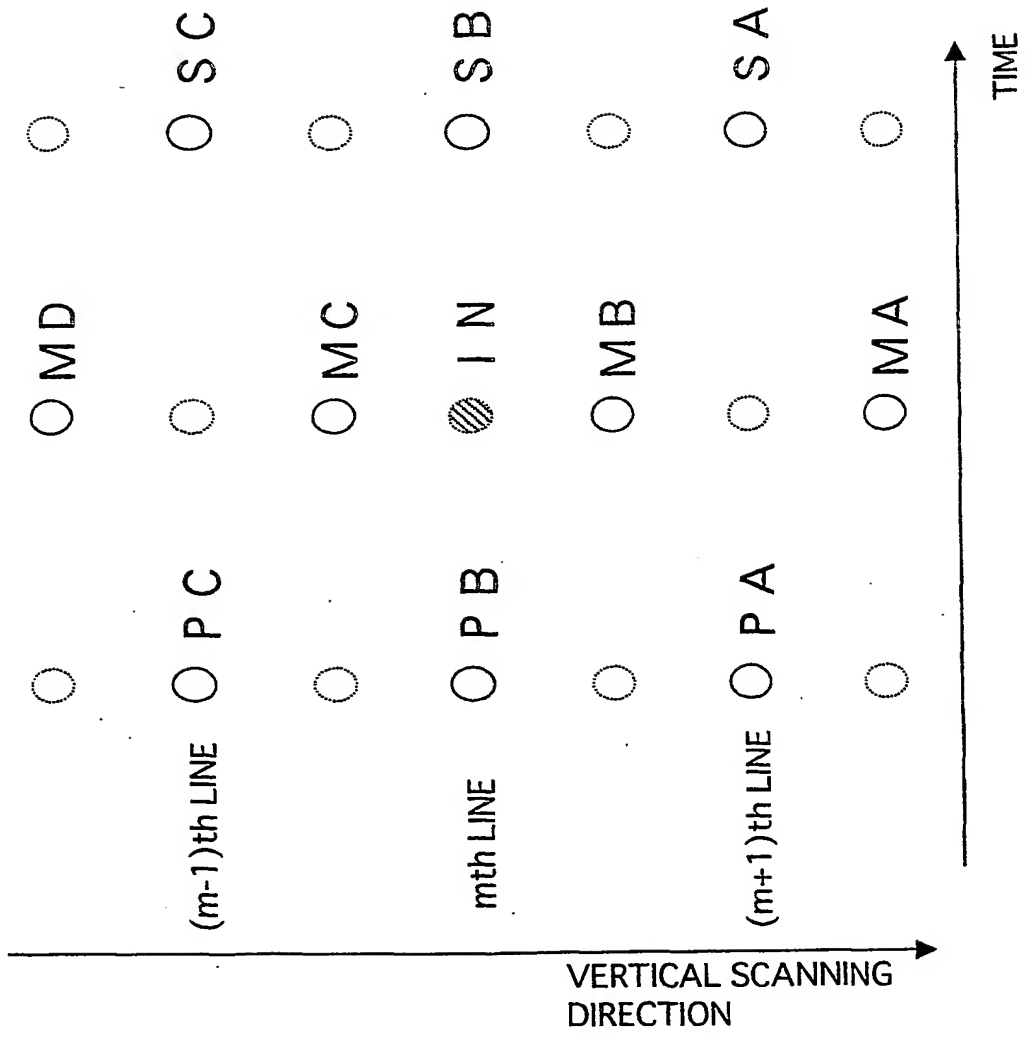


FIG.22

PB>M	PB>SB	M>SB	SELECT
1	0	0	a
0	1	1	a
1	1	1	b
0	0	0	b
1	1	0	c
0	0	1	c

M=(MB+MC)/2

INTERNATIONAL SEARCH REPORT

Int ›nal Application No
PCT/JP 01/09371

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N7/01 H04N5/44

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, IBM-TDB, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 975 156 A (SONY CORP) 26 January 2000 (2000-01-26) abstract; figures 2,3,17-20	1,10
A	page 3, line 5 -page 3, line 19	2-9, 11-21
Y	US 5 444 494 A (YAMAMOTO YUKINORI ET AL) 22 August 1995 (1995-08-22) figures 1-4	1,10
A		2-9, 11-21
Y	EP 0 586 262 A (TOKYO SHIBAURA ELECTRIC CO) 9 March 1994 (1994-03-09)	1
A	column 1, line 10 -column 1, line 31; figure 1	2-21

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
27 March 2002	08/04/2002

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Int ›nal Application No
PCT/JP 01/09371

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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